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NR31 0AG

Telephone +44 (0)1493 602602
Email:sales@midasdisplays.com
Email:tech@midasdisplays.com
www.midasdisplays.com

| MC42005A6W-FPTLWS-V2 | 4 x 20 | 5mm Character Height | LCD Module |
|---|---|---|---|
| **Specification** | | | |
| Version: 1 | | Date: 23/06/2021 | |
| **Revision** | | | |
| 1 | 22/06/2021 | First Issue | |

| Display Features | |
|---|---|
| Character Count | 4 x 20 |
| Appearance | Black on White |
| Logic Voltage | 5V |
| Interface | SPI |
| Font Set | English / Japanese |
| Display Mode | Transflective |
| Character Height | 4.75mm |
| LC Type | FSTN |
| Module Size | 98.00 x 60.00 x 13.60 mm |
| Operating Temperature | -20°C ~ +70°C |
| Construction | COB |
| LED Backlight | White |

RoHS compliant

| Box Quantity | Weight / Display |
|---|---|
| --- | --- |

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* - For full design functionality, please use this specification in conjunction with the RW1063 specification. (Provided Separately)

| Display Accessories | |
|---|---|
| **Part Number** | **Description** |
| MCCMDB-16SIL | LCD Interconnect board, can be driven from either a PC or a single Board computer with a USB output. |
| MCCBL1A16SLIP -16DILS-150 | 16 Way, Sinlge in-line to Dual In-line connector Cable. |
| MCCBL1A16SLIP -16SILS-150 | 16 Way, Single in-line to Single In-line connector Cable. |

| Optional Variants | | |
|---|---|---|
| **Fonts** | **Appearances** | **Voltage** |
| English/Japanese<br>English/Euro<br>English/Cyrillic | Black on Yellow/ Green<br>White on Blue<br>Black on White<br>Black on RGB | 3V<br>3.3V<br>5V |

# General Specification

The Features is described as follow:

- Module dimension: 98.0 x 60.0 x 13.6 (max.) mm
- View area: 77.0 x 25.2 mm
- Active area: 70.4 x 20.8 mm
- Number of Characters: 20 characters x 4 Lines
- Dot size: 0.55 x 0.55 mm
- Dot pitch: 0.60 x 0.60 mm
- Character size: 2.95 x 4.75 mm
- Character pitch: 3.55 x 5.35 mm
- LCD type: FSTN Positive Transflective
- Duty: 1/16
- View direction: 6 o'clock
- Backlight Type: LED ,White
- IC:RW1063
- Interface: 4-Line SPI

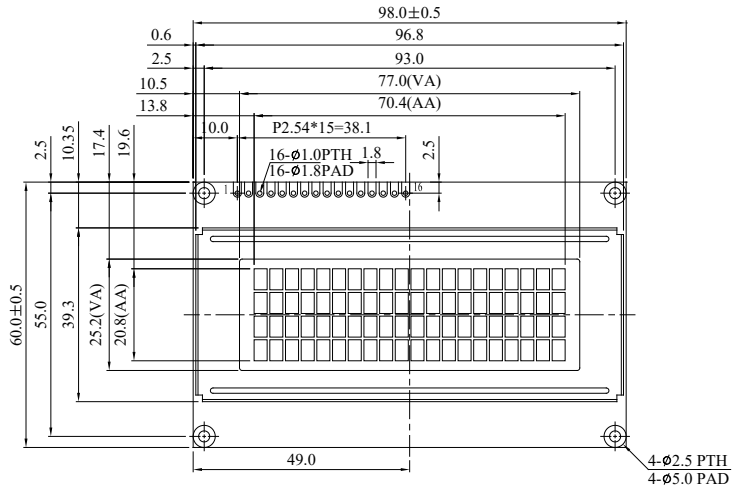
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# Interface Pin Function

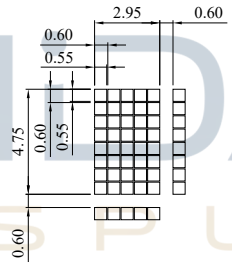
| Pin No. | Symbol | Level | Description |
|---|---|---|---|
| 1 | $V_{SS}$ | 0V | Ground |
| 2 | $V_{DD}$ | 5.0V | Supply Voltage for logic |
| 3 | VO | (Variable) | Operating voltage for LCD |
| 4 | RS | H/L | In bus mode, used as register selection input.<br>When RS = “High”, Date register is selected.<br>When RS = “Low”, Instruction register is selected. |
| 5 | NC | — | No connection |
| 6 | NC | — | No connection |
| 7 | NC | — | No connection |
| 8 | NC | — | No connection |
| 9 | NC | — | No connection |
| 10 | NC | — | No connection |
| 11 | NC | — | No connection |
| 12 | CSB | H/L | In 4-SPI serial mode, used as chip selection input.<br>When CSB = “Low”, selected<br>When CSB = “High”, not selected.<br>( Low access enable ) |
| 13 | SCLK | H/L | Serial clock input |
| 14 | SID | H/L | Serial data input |
| 15 | A | — | Power supply for B/L(+) |
| 16 | K | — | Power supply for B/L(-) |

MIDAS DISPLAYS DESIGN & MANUFACTURE SUPPLY

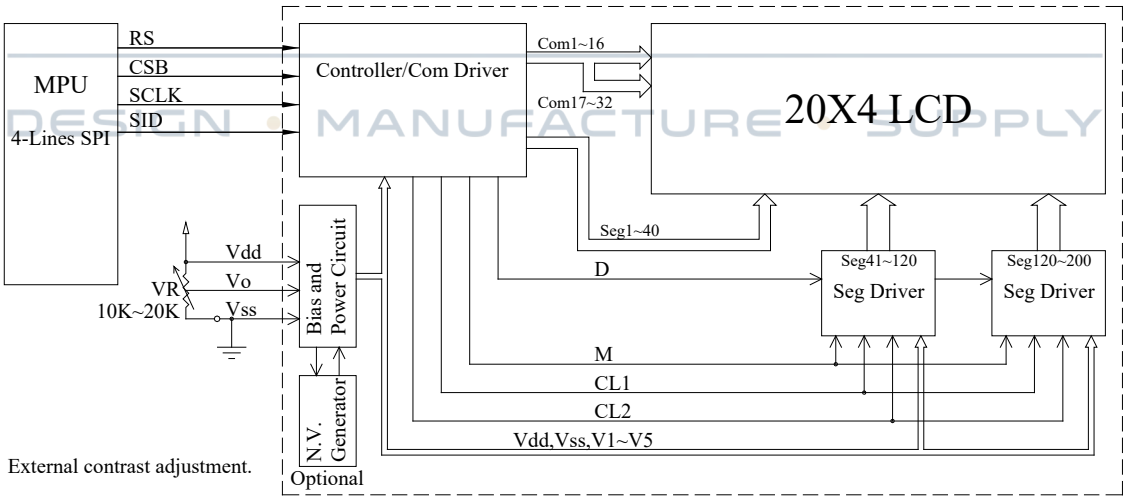
# Contour Drawing & Block Diagram




| PIN NO. | SYMBOL |
|---|---|
| 1 | Vss |
| 2 | Vdd |
| 3 | Vo |
| 4 | RS |
| 5 | NC |
| 6 | NC |
| 7 | NC |
| 8 | NC |
| 9 | NC |
| 10 | NC |
| 11 | NC |
| 12 | CSB |
| 13 | SCLK |
| 14 | SID |
| 15 | A |
| 16 | K |




The non-specified tolerance of dimension is ±0.3mm.




| Character located | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DDRAM address | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F | 10 | 11 | 12 | 13 |
| DDRAM address | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E | 4F | 50 | 51 | 52 | 53 |
| DDRAM address | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 |
| DDRAM address | 54 | 55 | 56 | 57 | 58 | 59 | 5A | 5B | 5C | 5D | 5E | 5F | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 |

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# Character Generator ROM Pattern

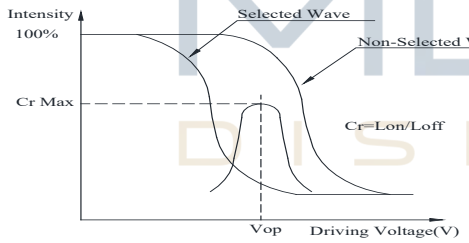
Table.2

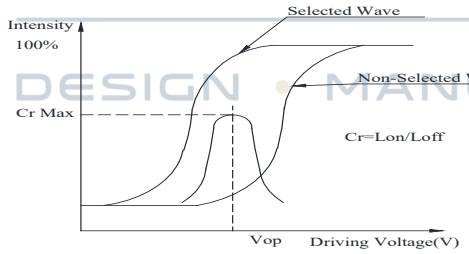


# Optical Characteristics

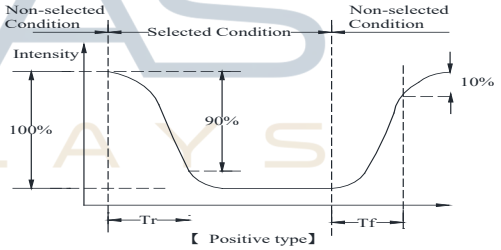
| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| View Angle | θ | CR≧2 | 0 | — | 30 | ψ= 180° |
| | θ | CR≧2 | 0 | — | 60 | ψ= 0° |
| | θ | CR≧2 | 0 | — | 45 | ψ= 90° |
| | θ | CR≧2 | 0 | — | 45 | ψ= 270° |
| Contrast Ratio | CR | — | — | 5 | — | — |
| Response Time | T rise | — | — | 150 | 200 | ms |
| | T fall | — | — | 150 | 200 | ms |

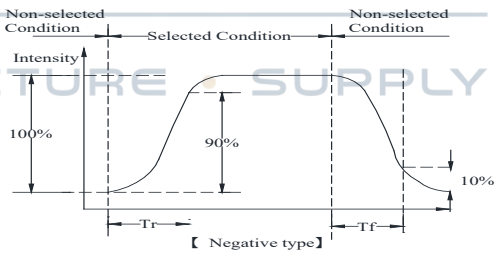
**Definition of Operation Voltage (Vop)**




**Definition of Response Time ( Tr , Tf )**



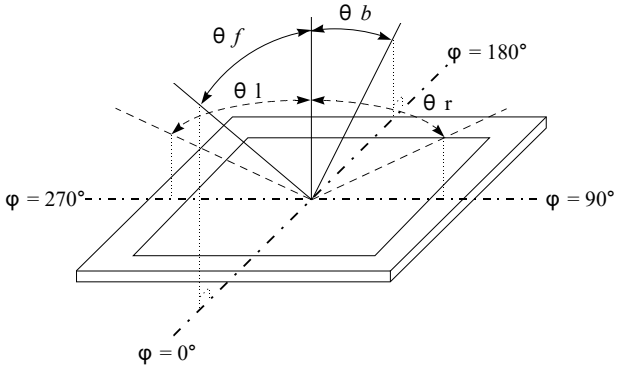




**Conditions :**

Operating Voltage : Vop  Viewing Angle(θ，φ) : 0°， 0°

Frame Frequency : 64 HZ Driving Waveform : 1/N duty , 1/a bias

**Definition of viewing angle(CR≧2)**




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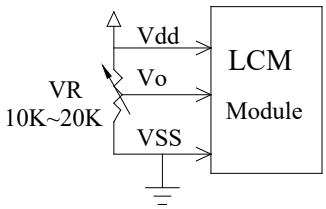
# Absolute Maximum Ratings

| Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Operating Temperature | $T_{OP}$ | -20 | — | +70 | ℃ |
| Storage Temperature | $T_{ST}$ | -30 | — | +80 | ℃ |
| Input Voltage | $V_{IN}$ | -0.3 | — | $V_{DD}$+0.3 | V |
| Supply Voltage For Logic | $V_{DD}$-$V_{SS}$ | -0.3 | — | 5.5 | V |
| Supply Voltage For LCD | $V_{DD}$-$V_0$ | $V_{SS}$ -0.3 | — | $V_{SS}$ +7.0 | V |

# Electrical Characteristics

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage For Logic | $V_{DD}$-$V_{SS}$ | — | 4.5 | 5.0 | 5.5 | V |
| Supply Voltage For LCD *Note | $V_{DD}$-$V_0$ | Ta=-20℃ | — | — | 5.3 | V |
| | | Ta=25℃ | 4.4 | 4.5 | 4.6 | V |
| | | Ta=70℃ | 3.8 | — | — | V |
| Input High Volt. | $V_{IH}$ | — | 2.5 | — | $V_{DD}$ | V |
| Input Low Volt. | $V_{IL}$ | — | -0.3 | — | 0.55 | V |
| Output High Volt. | $V_{OH}$ | — | 3.9 | — | $V_{DD}$ | V |
| Output Low Volt. | $V_{OL}$ | — | — | — | 0.4 | V |
| Supply Current | $I_{DD}$ | $V_{DD}$=5.0V | 1.0 | 1.2 | 1.5 | mA |

* Note: Please design the VOP adjustment circuit on customer's main board




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# Backlight Information

## Specification

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT | TEST CONDITION |
|---|---|---|---|---|---|---|
| Supply Current | ILED | 15 | 48 | 60 | mA | V=3.5V(Note 1) |
| Supply Voltage | V | 3.4 | 3.5 | 3.6 | V | — |
| Reverse Voltage | VR | — | — | 5 | V | — |
| Luminance (Without LCD) | IV | 448 | 560 | — | $CD/M^2$ | ILED=48mA |
| LED Life Time (For Reference only) | — | — | 50K | — | Hr. | ILED=48mA 25℃,50-60%RH, (Note 2) |
| Color | White | | | | | |

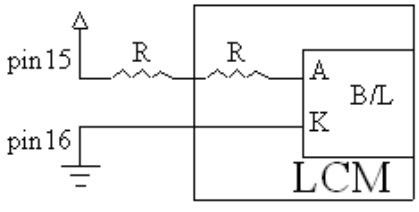
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**Note: The LED of B/L is drive by current only, drive voltage is for reference only. drive voltage can make driving current under safety area (current between minimum and maximum).**

**Note 1: Supply current minimum value is only for reference since LED brightness efficiency keeps enhancing. Current consumption becomes less and less to achieve the same luminance.**

**Note 2:50K hours is only an estimate for reference.**

2.Drive from pin15,pin16




(Will never get Vee output from pin15)

# Reliability

## Content of Reliability Test (Wide temperature, -20℃~70℃)

| Environmental Test | | | |
|---|---|---|---|
| **Test Item** | **Content of Test** | **Test Condition** | **Note** |
| High Temperature storage | Endurance test applying the high storage temperature for a long time. | 80℃<br>200hrs | 2 |
| Low Temperature storage | Endurance test applying the low storage temperature for a long time. | -30℃<br>200hrs | 1,2 |
| High Temperature Operation | Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time. | 70℃<br>200hrs | ——— |
| Low Temperature Operation | Endurance test applying the electric stress under low temperature for a long time. | -20℃<br>200hrs | 1 |
| High Temperature/ Humidity storage | The module should be allowed to stand at 60℃,90%RH max<br>For 96hrs under no-load condition excluding the polarizer,<br>Then taking it out and drying it at normal temperature. | 60℃,90%RH<br>96hrs | 1,2 |
| Thermal shock resistance | The sample should be allowed stand the following 10 cycles of operation<br>-20℃ 25℃ 70℃<br><br>30min 5min 30min<br>1 cycle | -20℃/70℃<br>10 cycles | ——— |
| Vibration test | Endurance test applying the vibration during transportation and using. | Total fixed amplitude : 1.5mm<br>Vibration Frequency : 10~55Hz<br>One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes | 3 |
| Static electricity test | Endurance test applying the electric stress to the terminal. | VS=±600V(contact), ±800v(air),<br>RS=330Ω<br>CS=150pF<br>10 times | ——— |

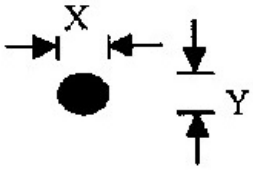
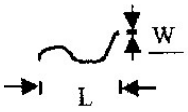
**Note1: No dew condensation to be observed.**

**Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.**

**Note3: The packing have to including into the vibration testing.**

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# Inspection specification

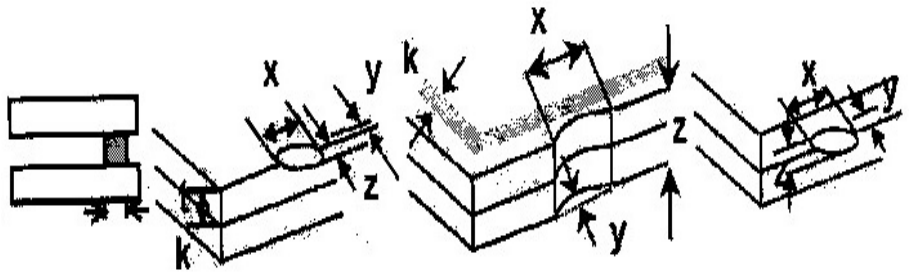
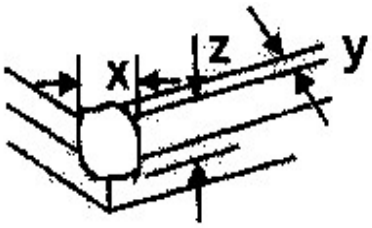
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>01</td><td>Electrical Testing</td><td>1.1 Missing vertical, horizontal segment, segment contrast defect.<br>1.2 Missing character , dot or icon.<br>1.3 Display malfunction.<br>1.4 No function or no display.<br>1.5 Current consumption exceeds product specifications.<br>1.6 LCD viewing angle defect.<br>1.7 Mixed product types.<br>1.8 Contrast defect.</td><td>0.65</td></tr>
<tr><td>02</td><td>Black or white spots on LCD (display only)</td><td>2.1 White and black spots on display ≦0.25mm, no more than three white or black spots present.<br>2.2 Densely spaced: No more than two spots or lines within 3mm</td><td>2.5</td></tr>
<tr><td rowspan="2">03</td><td rowspan="2">LCD black spots, white spots, contamination (non-display)</td><td>3.1 Round type : As following drawing<br>Φ=( x + y ) / 2
<table>
<tr><th>SIZE</th><th>Acceptable Q TY</th></tr>
<tr><td>Φ≦0.10</td><td>Accept no dense</td></tr>
<tr><td>0.10＜Φ≦0.20</td><td>2</td></tr>
<tr><td>0.20＜Φ≦0.25</td><td>1</td></tr>
<tr><td>0.25＜Φ</td><td>0</td></tr>
</table>

</td><td>2.5</td></tr>
<tr><td>3.2 Line type : (As following drawing)


<table>
<tr><th>Length</th><th>Width</th><th>Acceptable Q TY</th></tr>
<tr><td>---</td><td>W≦0.02</td><td>Accept no dense</td></tr>
<tr><td>L≦3.0</td><td>0.02＜W≦0.03</td><td rowspan="2">2</td></tr>
<tr><td>L≦2.5</td><td>0.03＜W≦0.05</td></tr>
<tr><td>---</td><td>0.05＜W</td><td>As round type</td></tr>
</table></td><td>2.5</td></tr>
</table>

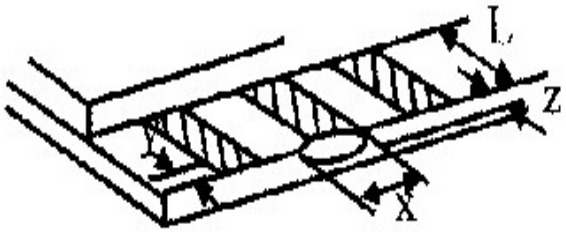
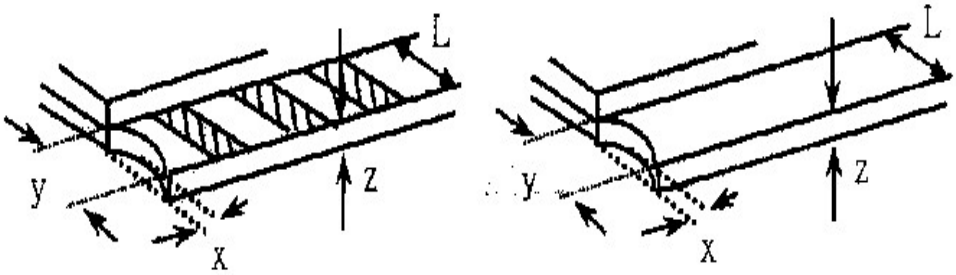
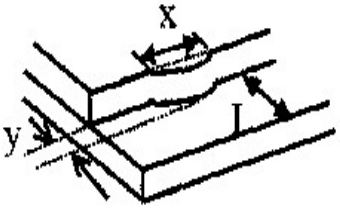
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<table>
<tr>
<td>04</td>
<td>Polarizer bubbles</td>
<td>If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction.
<table>
<tr><td>Size Φ</td><td>Acceptable Q TY</td></tr>
<tr><td>Φ≦0.20</td><td>Accept no dense</td></tr>
<tr><td>0.20＜Φ≦0.50</td><td>3</td></tr>
<tr><td>0.50＜Φ≦1.00</td><td>2</td></tr>
<tr><td>1.00＜Φ</td><td>0</td></tr>
<tr><td>Total Q TY</td><td>3</td></tr>
</table>
</td>
<td>2.5</td>
</tr>
</table>

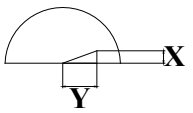
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<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>05</td><td>Scratches</td><td>Follow NO.3 LCD black spots, white spots, contamination</td><td></td></tr>
<tr><td>06</td><td>Chipped glass</td><td>Symbols Define:<br>x: Chip length y: Chip width z: Chip thickness<br>k: Seal width t: Glass thickness a: LCD side length<br>L: Electrode pad length:<br><br>6.1 General glass chip :<br>6.1.1 Chip on panel surface and crack between panels:<br><br><br><table><tr><th>z: Chip thickness</th><th>y: Chip width</th><th>x: Chip length</th></tr><tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr><tr><td>1/2t＜z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr></table>⊙If there are 2 or more chips, x is total length of each chip.<br><br>6.1.2 Corner crack:<br><br><br><table><tr><th>z: Chip thickness</th><th>y: Chip width</th><th>x: Chip length</th></tr><tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr><tr><td>1/2t＜z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr></table>⊙If there are 2 or more chips, x is the total length of each chip.</td><td>2.5</td></tr>
</table>

MIDAS DISPLAYS
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<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>06</td><td>Glass crack</td><td>
Symbols :<br>
x: Chip length y: Chip width z: Chip thickness<br>
k: Seal width t: Glass thickness a: LCD side length<br>
L: Electrode pad length<br>
6.2 Protrusion over terminal :<br>
6.2.1 Chip on electrode pad :<br>

<table>
<tr><th>y: Chip width</th><th>x: Chip length</th><th>z: Chip thickness</th></tr>
<tr><td>y≦0.5mm</td><td>x≦1/8a</td><td>0 ＜ z ≦ t</td></tr>
</table>
6.2.2 Non-conductive portion:<br>

<table>
<tr><th>y: Chip width</th><th>x: Chip length</th><th>z: Chip thickness</th></tr>
<tr><td>y≦ L</td><td>x≦1/8a</td><td>0 ＜ z ≦ t</td></tr>
</table>
⊙If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.<br>
⊙If the product will be heat sealed by the customer, the alignment mark not be damaged.<br>
6.2.3 Substrate protuberance and internal crack.<br>

<table>
<tr><th>y: width</th><th>x: length</th></tr>
<tr><td>y≦1/3L</td><td>x ≦ a</td></tr>
</table>
</td><td>2.5</td></tr>
</table>

DESIGN MANUFACTURE SUPPLY

| NO | Item | Criterion | AQL |
|---|---|---|---|
| 07 | Cracked glass | The LCD with extensive crack is not acceptable. | 2.5 |
| 08 | Backlight elements | 8.1 Illumination source flickers when lit.<br>8.2 Spots or scratched that appear when lit must be judged. Using LCD spot, lines and contamination standards.<br>8.3 Backlight doesn't light or color wrong. | 0.65<br>2.5<br>0.65 |
| 09 | Bezel | 9.1 Bezel may not have rust, be deformed or have fingerprints, stains or other contamination.<br>9.2 Bezel must comply with job specifications. | 2.5<br>0.65 |
| 10 | PCB、COB | 10.1 COB seal may not have pinholes larger than 0.2mm or contamination.<br>10.2 COB seal surface may not have pinholes through to the IC.<br>10.3 The height of the COB should not exceed the height indicated in the assembly diagram.<br>10.4 There may not be more than 2mm of sealant outside the seal area on the PCB. And there should be no more than three places.<br>10.5 No oxidation or contamination PCB terminals.<br>10.6 Parts on PCB must be the same as on the production characteristic chart. There should be no wrong parts, missing parts or excess parts.<br>10.7 The jumper on the PCB should conform to the product characteristic chart.<br>10.8 If solder gets on bezel tab pads, LED pad, zebra pad or screw hold pad, make sure it is smoothed down.<br>10.9 The Scraping testing standard for Copper Coating of PCB<br><br>X * Y<=2mm2 | 2.5<br>2.5<br>0.65<br>2.5<br>2.5<br>0.65<br>0.65<br>2.5<br>2.5 |
| 11 | Soldering | 11.1 No un-melted solder paste may be present on the PCB.<br>11.2 No cold solder joints, missing solder connections, oxidation or icicle.<br>11.3 No residue or solder balls on PCB.<br>11.4 No short circuits in components on PCB. | 2.5<br>2.5<br>2.5<br>0.65 |

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| NO | Item | Criterion | AQL |
|---|---|---|---|
| 12 | General appearance | 12.1 No oxidation, contamination, curves or, bends on interface Pin (OLB) of TCP. | 2.5 |
| | | 12.2 No cracks on interface pin (OLB) of TCP. | 0.65 |
| | | 12.3 No contamination, solder residue or solder balls on product. | 2.5 |
| | | 12.4 The IC on the TCP may not be damaged, circuits. | 2.5 |
| | | 12.5 The uppermost edge of the protective strip on the interface pin must be present or look as if it cause the interface pin to sever. | 2.5 |
| | | 12.6 The residual rosin or tin oil of soldering (component or chip component) is not burned into brown or black color. | 2.5 |
| | | 12.7 Sealant on top of the ITO circuit has not hardened. | 0.65 |
| | | 12.8 Pin type must match type in specification sheet. | 0.65 |
| | | 12.9 LCD pin loose or missing pins. | 0.65 |
| | | 12.10 Product packaging must the same as specified on packaging specification sheet. | 0.65 |
| | | 12.11 Product dimension and structure must conform to product specification sheet. | |
| | | 12.12 Visual defect outside of VA is not considered to be rejection. | |

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# Precautions in use of LCD Modules

(1)Avoid applying excessive shocks to the module or making any alterations or modifications to it.

(2)Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD module.

(3)Don't disassemble the LCM.

(4)Don't operate it above the absolute maximum rating.

(5)Don't drop, bend or twist LCM.

(6)Soldering: only to the I/O terminals.

(7)Storage: please storage in anti-static electricity container and clean environment.

(8) Midas have the right to change the passive components, including R3, R6 & backlight adjust resistors. (Resistors, capacitors, and other passive components will have different appearance and color caused by the different supplier.)

(9) Midas have the right to change the PCB Rev. (In order to satisfy the supplying stability, management optimization and the best product performance...etc, under the premise of not affecting the electrical characteristics and external dimensions, Midas have the right to modify the version.)

(10) To ensure the stability of the display screen, please apply screen saver after showing 30 mins of fixed display content.

(11)Please heat up a little the tape sticking on the components when removing it; otherwise the components might be damaged.

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# Material List of Components for RoHs

1. Midas hereby declares that all of or part of products (with the mark "#"in code), including, but not limited to, the LCM, accessories or packages, manufactured and/or delivered to your company (including your subsidiaries and affiliated company) directly or indirectly by our company (including our subsidiaries or affiliated companies) do not intentionally contain any of the substances listed in all applicable EU directives and regulations, including the following substances.

   Exhibit A：The Harmful Material List

| Material | Cd | Pb | Hg | Cr6+ | PBB | PBDE | DEHP | BBP | DBP | DIBP |
|---|---|---|---|---|---|---|---|---|---|---|
| Limited Value | **100 ppm** | **1000 ppm** | **1000 ppm** | **1000 ppm** | **1000 ppm** | **1000 ppm** | **1000 ppm** | **1000 ppm** | **1000 ppm** | **1000 ppm** |
| Above limited value is set up according to RoHS. | | | | | | | | | | |

2.Process for RoHS requirement：(only for RoHS inspection)

(1) Use the Sn/Ag/Cu soldering surface；the surface of Pb-free solder is rougher than we used before.

(2) Heat-resistance temp.：

Reflow：250℃,30 seconds Max.；

Connector soldering wave or hand soldering：320℃, 10 seconds max.

(3) Temp. curve of reflow, max. Temp.：235±5℃；

Recommended customer's soldering temp. of connector：280℃, 3 seconds.

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# Recommendable Storage

1. Place the panel or module in the temperature 25°C±5°C and the humidity below 65% RH
2. Do not place the module near organics solvents or corrosive gases.
3. Do not crush, shake, or jolt the module.

# Other (IC Information)

# 1.Function Description

**SYSTEM INTERFACE (Parallel 8-bit bus and 4-bit bus)**

This chip has all four kinds interface type with MPU: IIC, 4SPI, 4-bit bus and 8-bit bus. Serial and parallel buses (4-bit/8-bit) are selected by IF1 and IF0 input pins, and 4-bit bus and 8-bit bus is selected by DL bit in the instruction register.

During read or write operation, two 8-bit registers are used. One is data register (DR); the other is instruction register (IR). The data register (DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically.

So to speak, after MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically.

The Instruction register (IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.

IR: Instruction Register.

DR: Data Register.

| RS | R/W | **Operation** |
|---|---|---|
| 0 | 0 | Instruction write operation (MPU writes Instruction code into IR) |
| 0 | 1 | Read busy flag (DB7) and address counter (DB0 - DB6) |
| 1 | 0 | Data write operation (MPU writes data into DR |
| 1 | 1 | Data read operation (MPU reads data from DR) |

**BUSY FLAG (BF) (only support parallel 8-bit bus and 4-bit bus)**

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R / W = High (Read Instruction Operation); through DB7 before executing the next instruction, be sure that BF is not High.

**DISPLAY DATA RAM (DDRAM)**

DDRAM stores display data of maximum 80 x 8 bits (80 characters). DDRAM address is set in the address counter (AC) as a hexadecimal number. (Refer to Figure 1.)

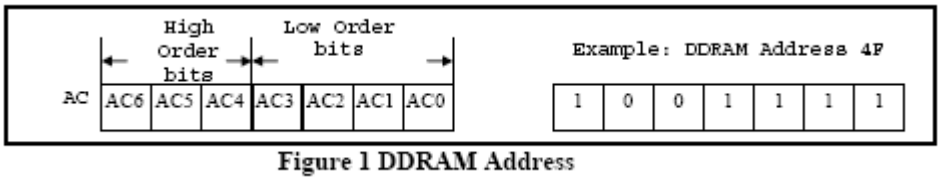



Figure 1 DDRAM Address

Since DDRAM has 8 bits data. It is possible to access 256 CGROM/CGRAM fonts.

**1-line display (N = 0) (Figure 2)**

When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the Controller, 8 characters are displayed. See Figure 3.

When the display shift operation is performed, the DDRAM address shifts. See Figure 3.

| Display Position (Digit) | 1 | 2 | 3 | 4 | 5 | 6 | ..... | 78 | 79 | 80 |
|---|---|---|---|---|---|---|---|---|---|---|
| DDRAM Address | 00 | 01 | 02 | 03 | 04 | 05 | ..... | 4D | 4E | 4F |

**Figure 2 1-Line Display**

| Display Position | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| DDRAM Address | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 |
| For Shift Left | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 |
| For Shift Right | 4F | 00 | 01 | 02 | 03 | 04 | 05 | 06 |

**Figure 3 1-Line by 8-Character Display Example**

**2-line display (N = 1) (Figure 4)**

Case 1: When the number of display characters is less than 40 x 2 lines, the two lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when just the Controller is used, 8 characters x □2 lines are displayed. See Figure 5.

When display shift operation is performed, the DDRAM address shifts. See Figure 5.

| Display Position | 1 | 2 | 3 | 4 | 5 | 6 | ..... | 38 | 39 | 40 |
|---|---|---|---|---|---|---|---|---|---|---|
| DDRAM Address | 00 | 01 | 02 | 03 | 04 | 05 | ..... | 25 | 26 | 27 |
| (hexadecimal) | 40 | 41 | 42 | 43 | 44 | 45 | ..... | 65 | 66 | 67 |

**Figure 4 2-Lines Display**

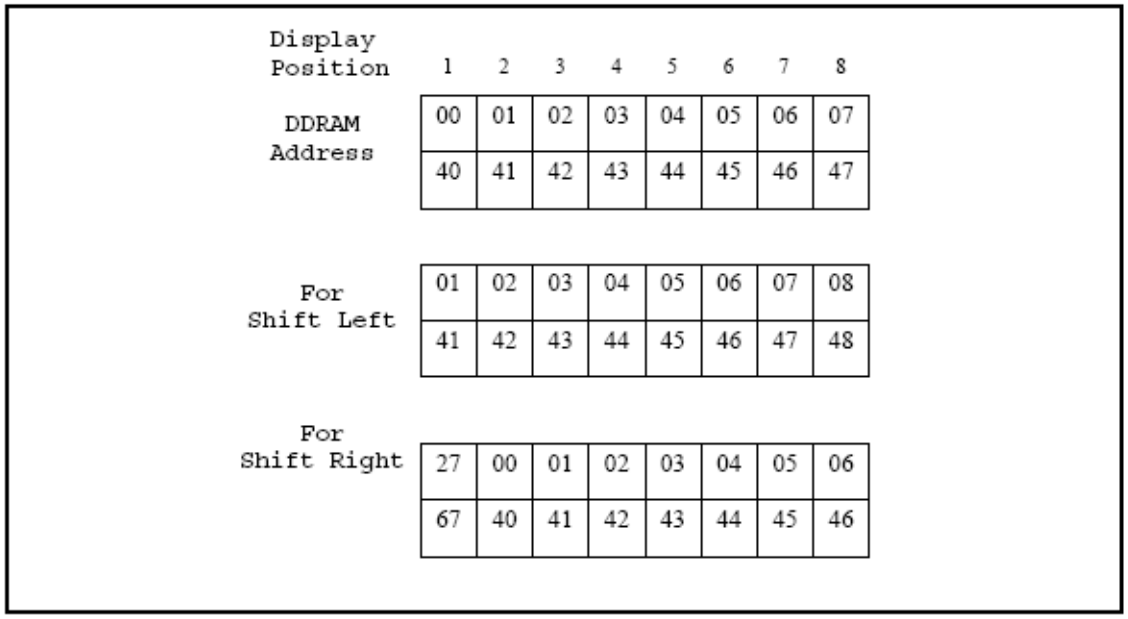



**Figure 5 2-Lines by 8-Character Display Example**

Case 2: For a 16-character x □2-line display, the Controller can be extended using one 40-output extension driver. See Figure 6.

When display shift operation is performed, the DDRAM address shifts. See Figure 6.

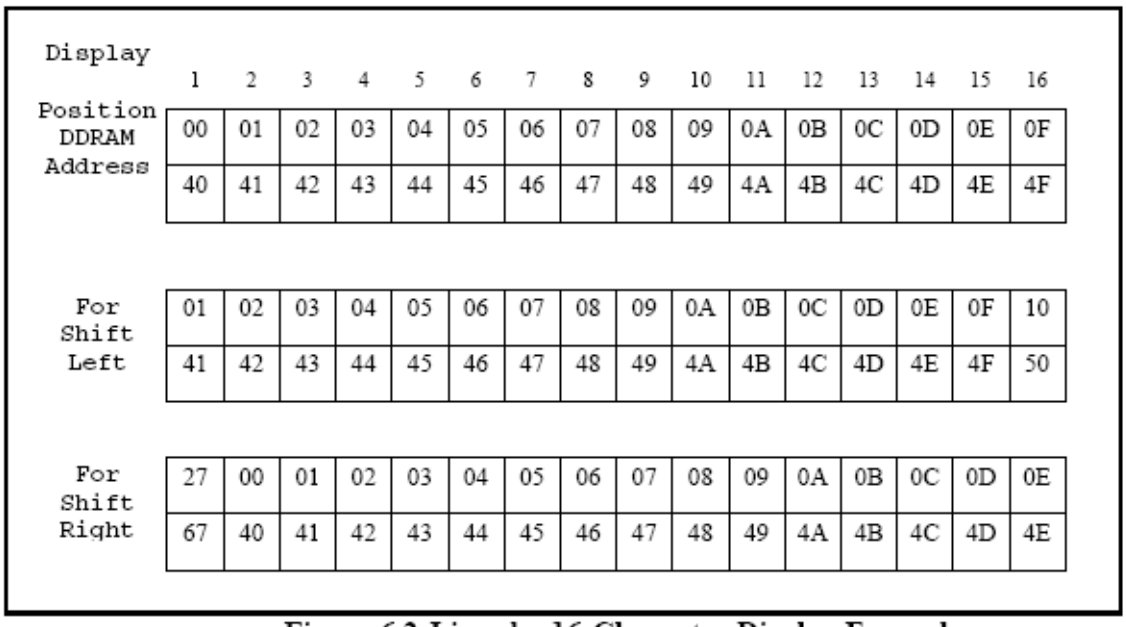



**Figure 6 2-Lines by 16-Character Display Example**

**TIMING GENERATION CIRCUIT**

Timing generation circuit generates clock signals for the internal operations.

**ADDRESS COUNTER (AC)**

Address Counter (AC) stores DDRAM/CGRAM address, transferred from IR.

After writing into (reading from) DDRAM/CGRAM/SEGRAM, AC is automatically increased (decreased) by 1.

When RS = "Low" and R/W = "High", AC can be read through DB0-DB6

**CURSOR/BLINK CONTROL CIRCUIT**

It controls cursor/blink ON/OFF and black/white inversion at cursor position.

**LCD DRIVER CIRCUIT**

LCD Driver circuit has 16 common and 40 segment signals for 2-line display (N=1) or 8 common and 40 segments for 1-line display (N=0) for LCD driving.

Data from CGRAM/CGROM is transferred to 40 bit segment latches serially, and then it is stored to 40 bit shift latch.

**CGROM (CHARACTER GENERATOR ROM)**

CGROM has 10,240 bits (256 characters x 5 x 8 dot)

**CGRAM (CHARACTER GENERATOR RAM)**

CGRAM has up to 5 □□8 dots 8 characters. By writing font data to CGRAM, user defined character can be used (refer to Table 2).

**5** x **8 dots Character Pattern**

**Table 2. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)**

| Character Code (DDRAM data) | | | | | | | | CGRAM Address | | | | | | CGRAM Data | | | | | | | | Pattern Number |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | A5 | A4 | A3 | A2 | A1 | A0 | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | X | X | 0 | 1 | 1 | 1 | 0 | Pattern 1 |
| - | - | - | - | - | 0 | 0 | 0 | - | - | - | 0 | 0 | 1 | - | - | - | 1 | 0 | 0 | 0 | 1 | |
| - | - | - | - | - | 0 | 0 | 0 | - | - | - | 0 | 1 | 0 | - | - | - | 1 | 0 | 0 | 0 | 1 | |
| - | - | - | - | - | 0 | 0 | 0 | - | - | - | 0 | 1 | 1 | - | - | - | 1 | 1 | 1 | 1 | 1 | |
| - | - | - | - | - | 0 | 0 | 0 | - | - | - | 1 | 0 | 0 | - | - | - | 1 | 0 | 0 | 0 | 1 | |
| - | - | - | - | - | 0 | 0 | 0 | - | - | - | 1 | 0 | 1 | - | - | - | 1 | 0 | 0 | 0 | 1 | |
| - | - | - | - | - | 0 | 0 | 0 | - | - | - | 1 | 1 | 0 | - | - | - | 1 | 0 | 0 | 0 | 1 | |
| - | - | - | - | - | 0 | 0 | 0 | - | - | - | 1 | 1 | 1 | - | - | - | 0 | 0 | 0 | 0 | 0 | |
| | | | | - | | | | | | - | | | - | | | | | - | | | | |
| | | | | - | | | | | | - | | | - | | | | | - | | | | |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | X | X | X | 1 | 0 | 0 | 0 | 1 | Pattern 8 |
| - | - | - | - | - | 1 | 1 | 1 | - | - | - | 0 | 0 | 1 | - | - | - | 1 | 0 | 0 | 0 | 1 | |
| - | - | - | - | - | 1 | 1 | 1 | - | - | - | 0 | 1 | 0 | - | - | - | 1 | 0 | 0 | 0 | 1 | |
| - | - | - | - | - | 1 | 1 | 1 | - | - | - | 0 | 1 | 1 | - | - | - | 1 | 1 | 1 | 1 | 1 | |
| - | - | - | - | - | 1 | 1 | 1 | - | - | - | 1 | 0 | 0 | - | - | - | 1 | 0 | 0 | 0 | 1 | |
| - | - | - | - | - | 1 | 1 | 1 | - | - | - | 1 | 0 | 1 | - | - | - | 1 | 0 | 0 | 0 | 1 | |
| - | - | - | - | - | 1 | 1 | 1 | - | - | - | 1 | 1 | 0 | - | - | - | 1 | 0 | 0 | 0 | 1 | |
| - | - | - | - | - | 1 | 1 | 1 | - | - | - | 1 | 1 | 1 | - | - | - | 0 | 0 | 0 | 0 | 0 | |

Notes:

1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).
2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor. Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display. If the 8th line data is 1, 1 bit will light up the 8th line regardless of the cursor presence.

3. Character pattern row positions correspond to CGRAM data bits 0 to 4 (bit 4 being at the left).
4. As shown Table 2, CGRAM character patterns are selected when character code bits 4 to 7 are all 0 and MW=0. However, since character code bit 3 has no effect, the H display example above can be selected by either character code 00H or 08H.
5. 1 for CGRAM data corresponds to display selection and 0 to non-selection.
"-": Indicates no effect.

# 2.Instruction Table

| Instruction | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Description | Description Time (540KHz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Read display data | 1 | 1 | Read data | | | | | | | | Read data into DDRAM/CGRAM/SEGRAM | 18.5us |
| Write display data | 1 | 0 | Write data | | | | | | | | Write data into DDRAM/CGRAM/SEGRAM | 18.5us |
| Clear Display | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Write "20H" to DDRAM, and set DDRAM address to "00H" from AC | 0.76ms |
| Return Home | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed. | 0.76ms |
| Entry Mode Set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S | Assign cursor moving direction and specify display shift. These operations are performed during data read and write.<br>I/D="1": increment<br>I/D="0": decrement | 18.5us |
| Display ON/OFF | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | Set Display /Cursor/Blink On/OFF<br>D="1": display on<br>D="0": display off<br><br>C="1": cursor on<br>C="0": cursor off<br><br>B="1": blink on<br>B="0": blink off | 18.5us |
| Cursor or Display shift | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | X | X | Cursor or display shift<br>S/C="1": display shift<br>S/C="0": cursor shift<br><br>R/L="1": shift to right<br>R/L="0": shift to left | 18.5us |
| Function Set | 0 | 0 | 0 | 0 | 1 | DL | N | F | X | X | Set Interface Data Length<br>DL= 8-bit interface/ 4-bit interface<br>N = 2-line/1-line display<br>F= 5x8 Font Size / 5x11Font Size | 18.5us |
| Set CGRAM Address | 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set CGRAM address in address counter | 18.5us |
| Set DDRAM Address | 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set DDRAM address in address counter | 18.5us |
| Read Busy Flag and Address | 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Can know internal operation is ready or not by reading BF.<br>The contents of address counter can also be read.<br>BF="1": busy state<br>BF="0": ready state | 0us |

**Clear Display**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status; namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

**Return Home:**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | X |

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. A content of DDRAM does not change.

**Entry Mode Set:**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S |

Set the moving direction of cursor and display.

**I/D: Increment/decrement of DDRAM address (cursor or blink)**

I/D = 1: cursor/blink moves to right and DDRAM address is increased by 1.

I/D = 0: cursor/blink moves to left and DDRAM address is decreased by 1.

* CGRAM operates the same as DDRAM, when read/write from or to CGRAM

**S: Shift of entire display**

When DDRAM read (CGRAM read/write) operation or S = "Low", shift of entire display is not performed.

If S= "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = "1": shift left, I/D = "0": shift right).

| S | I/D | Description |
|---|---|---|
| H | H | Shift the display to the left |
| H | L | Shift the display to the right |

**Display ON/OFF**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B |

Control display/cursor/blink ON/OFF 1 bit register.

**D: Display ON/OFF control bit.**

D = 1: entire display is turned on.

D = 0: display is turned off, but display data is remained in DDRAM.

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**C: Cursor ON/OFF control bit.**

C = 1: cursor is turned on.

C = 0: cursor is disappeared in current display, but I/D register remains its data.

**B: Cursor Blink ON/OFF control bit.**

B = 1: cursor blink is on, that performs alternate between all the high data and display character at the cursor position. If fosc has 540 kHz frequency, blinking has 185 ms interval.

B = 0: blink is off.

**Cursor or Display Shift**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | - | - |

Without writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data (refer to Table 4). During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line.

Note that display shift is performed simultaneously by the shift enable instruction. When displayed data is shifted repeatedly, all display lines shifted simultaneously. When display shift is performed, the contents of address counter are not changed.

**Table 4. Shift Patterns According to S/C and R/L Bits**

| S/C | R/L | Operation |
|---|---|---|
| 0 | 0 | Shift cursor to the left, address counter is decreased by 1 |
| 0 | 1 | Shift cursor to the right, address counter is increased by 1 |
| 1 | 0 | Shift all the display to the left, cursor moves according to the display |
| 1 | 1 | Shift all the display to the right, cursor moves according to the display |

**Function Set**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | DL | N | F | X | X |

**DL: Interface data length control bit**

When DL = "High", it means 8-bit bus mode with MPU.

When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.

When 4-bit bus mode, it needs to transfer 4-bit data by two times.

IF using IIC and 4-SPI interface、DL bit must be setting to “1”

**N: Display line number control bit**

When N = "Low", it means 1-line display mode.

When N = "High", 2-line display mode is set.

**F: Display font type control bit**

When F = "Low", it means 5 x 8 dots format display mode

When F = "High", 5 x11 dots format display mode.

| N | F | No. of Display Lines | Character Font | Duty Factor |
|---|---|---|---|---|
| L | L | 1 | 5x8 | 1/8 |
| L | H | 1 | 5x11 | 1/11 |
| H | x | 2 | 5x8 | 1/16 |

**Set CGRAM Address**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Set CGRAM address to AC.
This instruction makes CGRAM data available from MPU.

**Set DDRAM Address**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU.
When 1-line display mode (N=0), DDRAM address is from “00H” to “4FH”
In 2-line display mode (NW = 0), DDRAM address in the 1st line is from "00H" - "27H", and DDRAM address in the 2nd line is from "40H" - "67H".

**Read Busy Flag and Address** (only support parallel 8-bit bus and 4 bit bus)

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

This instruction shows whether Controller is in internal operation or not. If the resultant BF is “high”, it means the internal operation is in progress and you have to wait until BF to be Low, and then the next instruction can be performed. In this instruction you can read also the value of address counter.

**Write Data to RAM**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Write binary 8-bit data to DDRAM/CGRAM/SEGRAM.
The selection of RAM from DDRAM, CGRAM, is set by the previous address set instruction: DDRAM address set, CGRAM address set. RAM set instruction can also determine the AC direction to RAM.
After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

**Read Data from RAM** (only support parallel 8-bit bus and 4 bit bus)

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Read binary 8-bit data from DDRAM/CGRAM.
The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined.
If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data.
In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction: it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode.
After CGRAM read operation, display shift may not be executed correctly.
* In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

MIDAS DISPLAYS
DESIGN MANUFACTURE SUPPLY

**OUTLINE**
To overcome the speed difference between internal clock of Controller and MPU clock, Controller performs internal operation by storing control information to IR (Instruction Register) or DR (data Register).
The internal operation is determined according to the signal from MPU, composed of read/write and data bus.
I Nstruction can be divided largely four kinds;
*Controller function set instructions (set display methods, set data length, etc.)
*Address set instructions to internal RAM
*Data transfer instructions with internal RAM
*Others
The address of internal RAM is automatically increased or decreased by 1.
**NOTE:** During internal operation, Busy Flag (DB7) is read high. Busy Flag check must be preceded the next instruction.
Busy flag check must be proceeded the next instruction.
When an MPU program with Busy Flag (DB7) checking is made, 1/2 Fosc (is necessary) for executing the next instruction by the falling edge of the “E” signal after the Busy Flag (DB7) goes to “Low”.

## INTERFACE WITH MPU

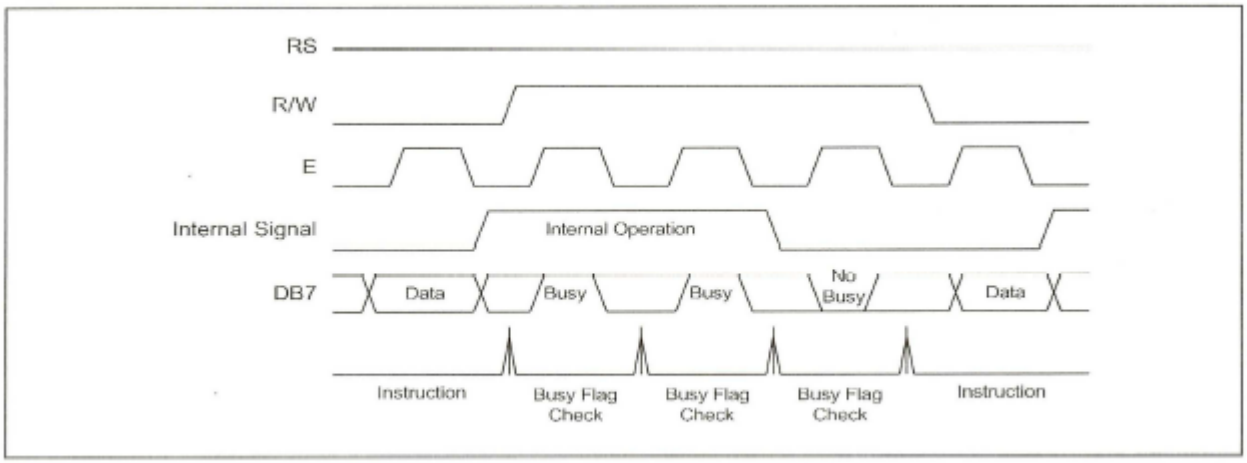
Controller can transfer data in bus mode (4-bit or 8-bit) or serial mode with MPU.
In case of 4-bit bus mode, data transfer is performed by two times to transfer 1 byte data.
□□When interfacing data lengths are 4-bit, only 4 ports, from DB4 - DB7, are used as data bus. At first higher 4-bit (in case of 8-bit bus mode, the contents of DB4 - DB7) are transferred, and then lower 4- bit (in case of 8-bit bus mode, the contents of DB0 - DB3) are transferred. So transfer is performed by two times.
Busy Flag outputs "High" after the second transfer are ended.
□□When interfacing data length are 8-bit, transfer is performed at a time through 8 ports, from DB0 - DB7.
□□Interface is selected by IF1,IF0 pins (refer to **Bonding Note for IF1, IF0** on Page 10)

| IF1 | IF0 | Interface select |
|---|---|---|
| open | open | 6800 8/4 bit |
| open | Bonding to VDD | IIC |
| Bonding to VDD | open | 4-line SPI |

## INTERFACE WITH MPU IN BUS MODE

### Interface with 8-bit MPU

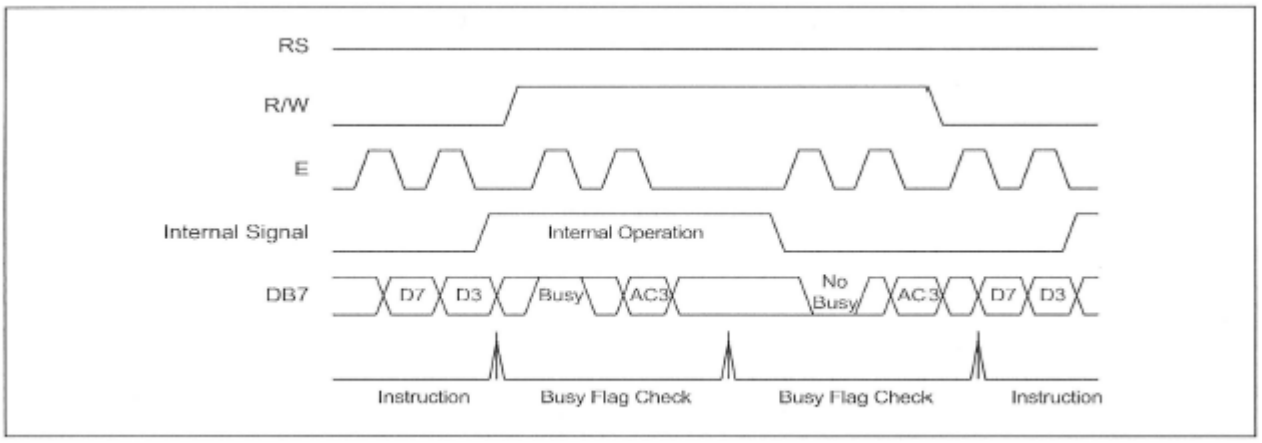
If 8-bits MPU is used, Controller can connect directly with that. In this case, port E, RS, R/W and DB0 to DB7 need to interface each other. Example of timing sequence is shown below.




**Example of 8-bit Bus Mode Timing Sequence**

### Interface with 4-bit MPU

If 4-bit MPU is used, Controller can connect directly with this. In this case, port E, RS, R/W and DB4 - DB7 need to interface each other. The transfer is performed by two times. Example of timing sequence is shown below.

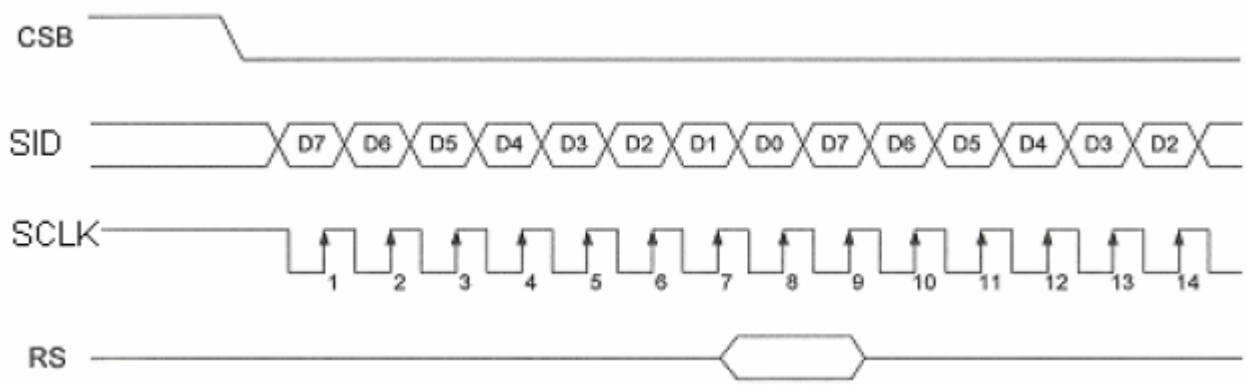



**Example of 4-bit Bus Mode Timing Sequence**

**For serial interface data, bus lines (DB5 to DB7) are used. 4-Line SPI**

If 4-Pin SPI mode is used, CSB (DB5), SID (DB7), SCLK (DB6), and RS are used. They are chip selection; serial input data, serial clock input, and data/instruction section, relatively. The example of timing sequence is shown below.

**Example of timing sequence**




Note: Following is the master SPI clock mode of MPU.

Idle state for clock is a high level，data transmitted on rising edge of SCLK, and data is hold during low level.

**For serial interface data, bus lines (DB5(CSB)、DB6(SDA) and DB7(SCL)) are used.**

**IIC interface**

The IIC interface receives and executes the commands sent via the IIC Interface. It also receives RAM data and sends it to the RAM.

The IIC Interface is for bi-directional, two-line communication between different ICs or modules.

Serial data line

SDA (DB6) and a Serial clock line SCL (DB7) must be connected to a positive supply via a pull-up resistor.

Data transfer may be initiated only when the bus is not busy.

*The CSB (DB5) Pin must be setting to “VSS”.

* When IIC interface is selected, the DL register must be set to “1”.

**BIT TRANSFER**

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the
HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control
signal. Bit transfer is illustrated in Fig.9.1

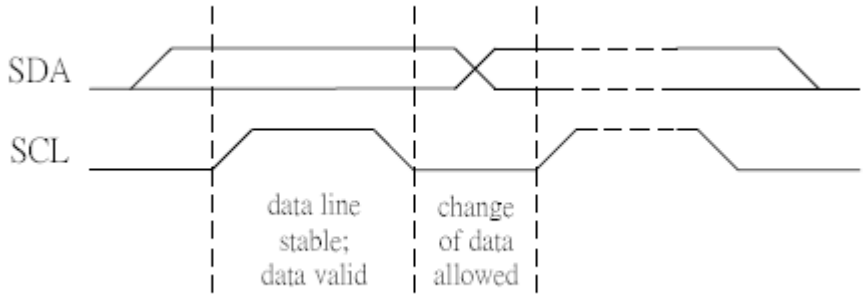



**Fig .9.1 Bit transfer**

**START AND STOP CONDITIONS**

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in
Fig.9.2

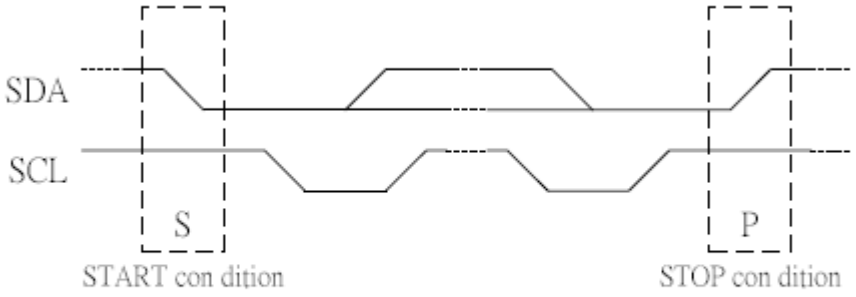



**Fig .9.2 Definition of START and STOP conditions**

**SYSTEM CONFIGURATION**

The system configuration is illustrated in Fig.9.3

· Transmitter: the device, which sends the data to the bus

· Receiver: the device, which receives the data from the bus

· Master: the device, which initiates a transfer, generates clock signals and terminates a transfer

· Slave: the device addressed by a master

· Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message

· Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
· Synchronization: procedure to synchronize the clock signals of two or more devices.

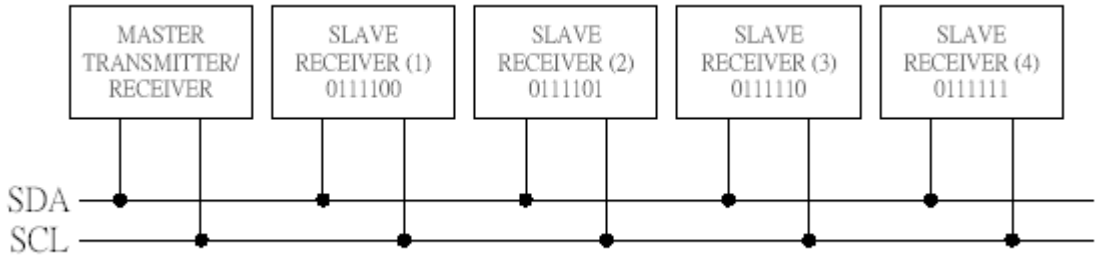


Fig .9.3 System configuration

**ACKNOWLEDGE**

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an Acknowledge after the reception of each byte. A master receiver must also generate an Acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the Acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an Acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the IIC
Interface is illustrated in Fig.9.4

MIDAS DISPLAYS
DESIGN • MANUFACTURE • SUPPLY

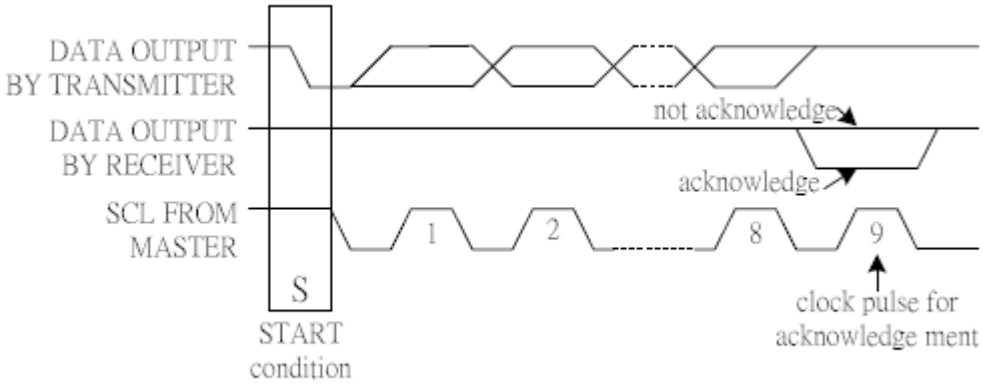


Fig .9.4 Acknowledgement on the 2-line Interface

**IIC Interface protocol**

The Controller supports command, data write addressed slaves on the bus.
Before any data is transmitted on the IIC Interface, the device, which should respond, is addressed first.
Four 7-bit slave addresses (0111100, 0111101, 0111110 and 0111111) are reserved for the

Controller. The least significant bit of the slave address is set by connecting the input SA0 (DB0) and SA1 (DB1) to either logic 0 (VSS) or logic 1 (VDD).
The IIC Interface protocol is illustrated in Figure.9.5
The sequence is initiated with a START condition (S) from the IIC Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the IIC Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.
A command word consists of a control byte, which defines Co and A0, plus a data byte.
The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the A0 bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the A0 bit setting; either a series of display data bytes or command data bytes may follow. If the A0 bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended Controller device. If the A0 bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the IIC interface-bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

MIDAS DISPLAYS

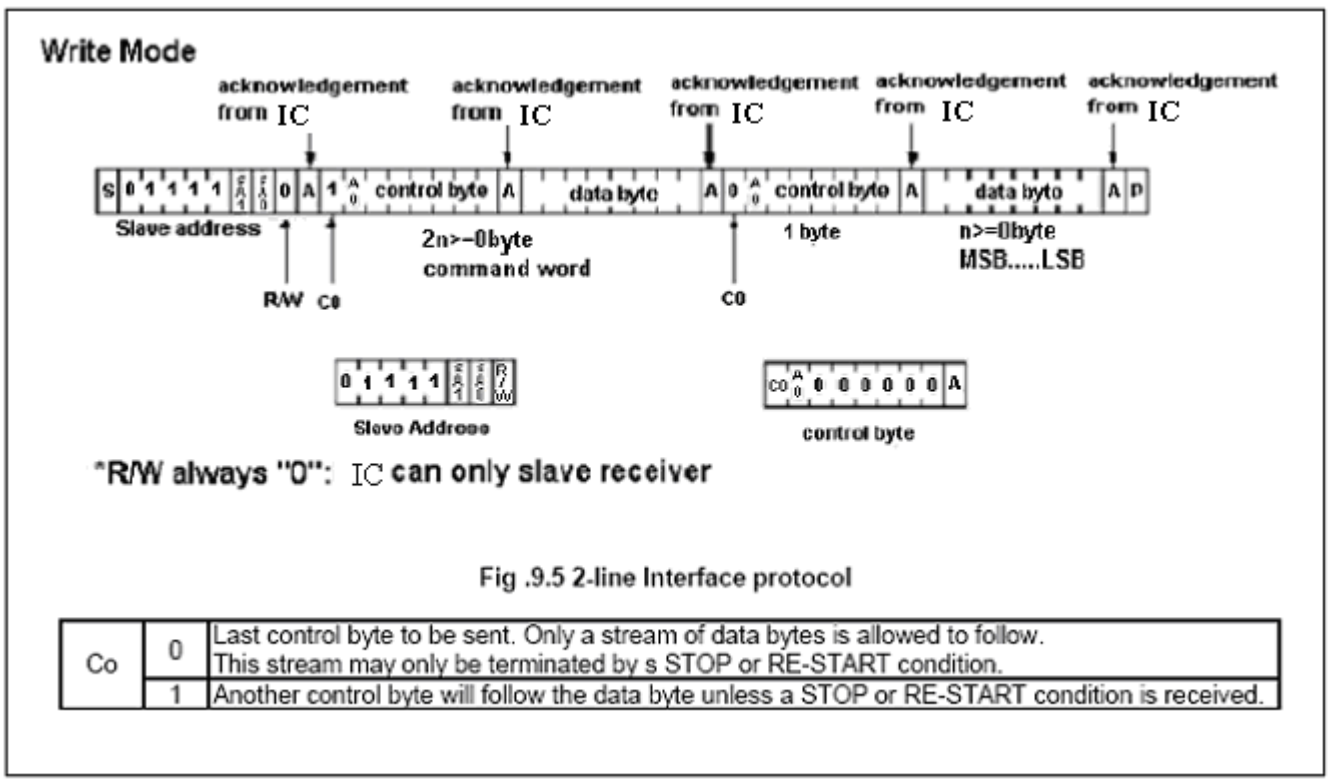



Fig .9.5 2-line Interface protocol

| | | |
|---|---|---|
| Co | 0 | Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by s STOP or RE-START condition. |
| | 1 | Another control byte will follow the data byte unless a STOP or RE-START condition is received. |

**INITIALIZING**

**INITIALIZING BY INTERNAL RESET CIRCUIT**

When the power is turned on, Controller is initialized automatically by power on reset circuit. During the initialization, the following instructions are executed, and BF (Busy Flag) is kept "High"(busy state) to the end of initialization.

**Clear Display Instruction**

Write "20H" to all DDRAM

**Set Functions Instruction**

DL = 1: 8-bit bus mode

N = 0: 1-line display

F = 0: 5 x 8 dot character font

**Display ON/OFF Instruction**

D = 0: Display OFF

C = 0: Cursor OFF

B = 0: Blink OFF

**Set Entry Mode Instruction**

I/D = 1: Increment by 1

S = 0: No entire display shift

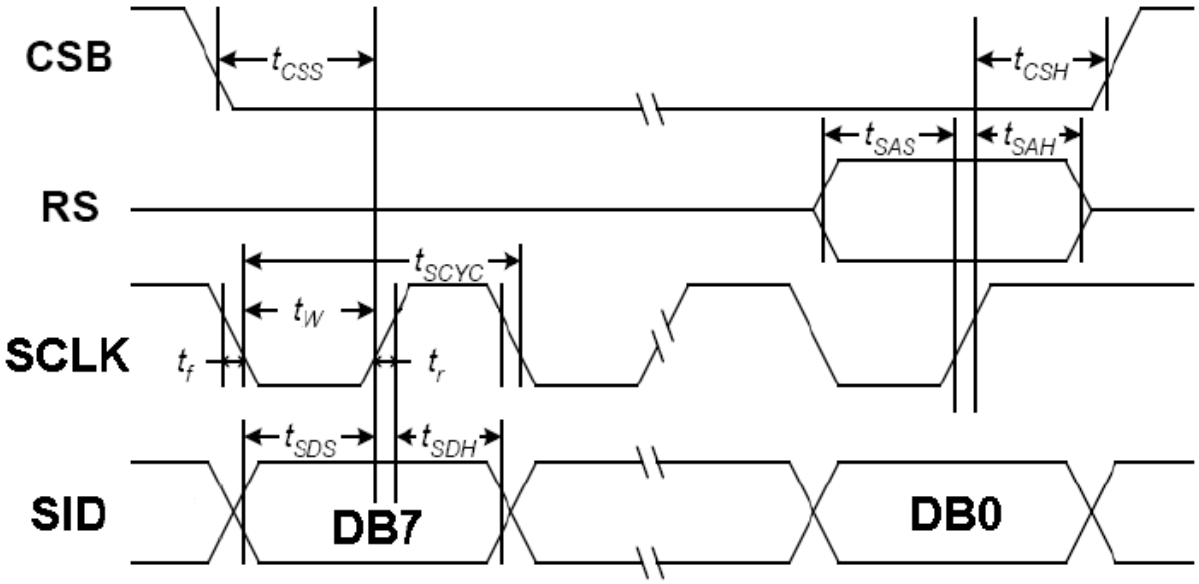
Note:

If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the Controller. For such a case, initialization must be performed by the MPU as explain by the following figure.

MIDAS DISPLAYS
DESIGN • MANUFACTURE • SUPPLY

# 3.Timing Characteristics

**Serial interface timing (4-SPI)**




MIDAS DISPLAYS

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**In 4-SPI Serial Interface (TA = 25℃, VCC = 2.7V )**

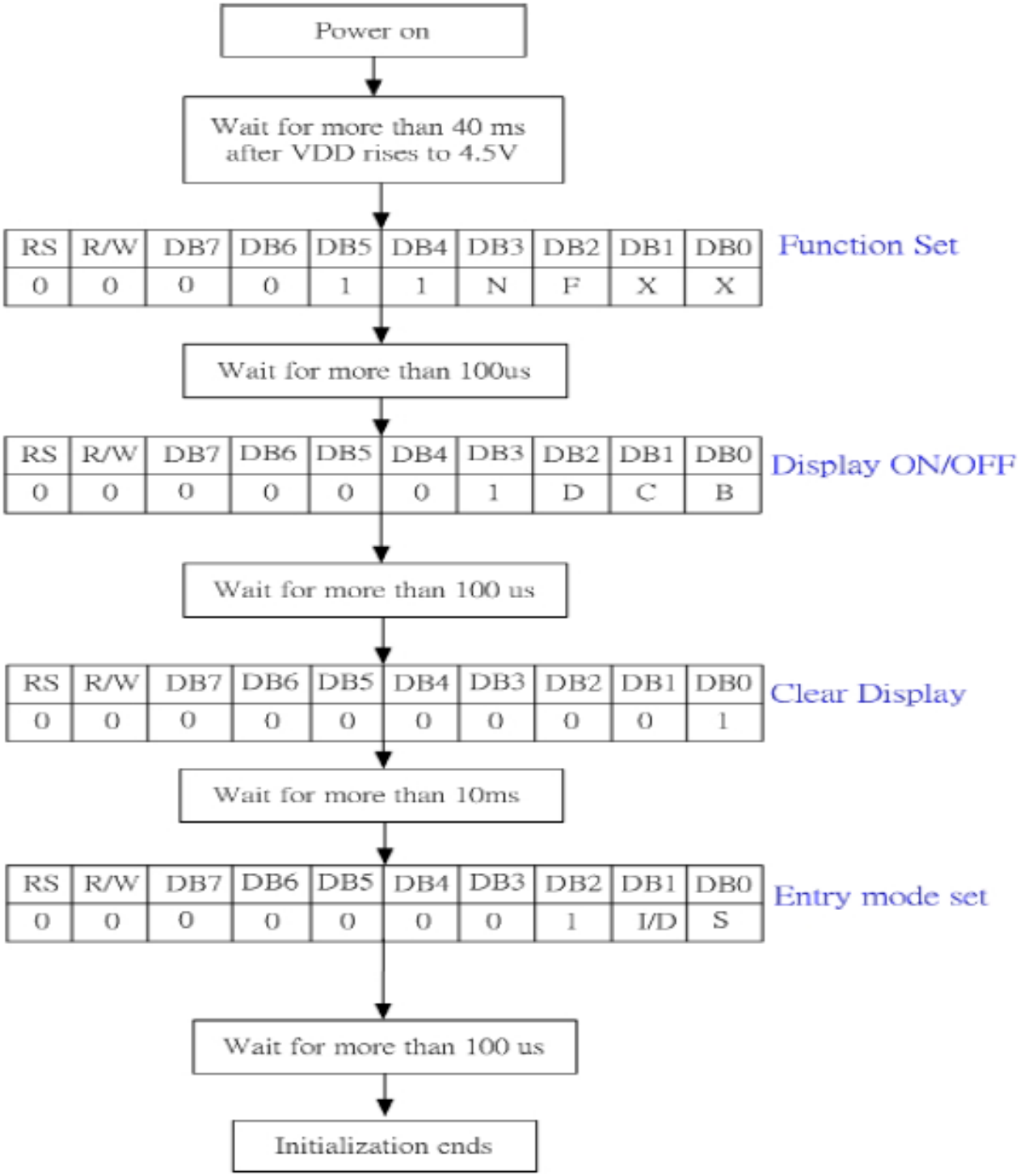
| Symbol | Characteristics | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| *Write Mode (Writing data from MPU to RW1063)* | | | | | | |
| $t_{SCYC}$ | SCLK Cycle Time | SCLK | 640 | - | - | ns |
| $t_w$ | SCLK pulse width | SCLK | 320 | - | - | ns |
| $t_R$,$t_F$ | SCLK Rise/Fall time | SCLK | - | - | 25 | ns |
| $t_{SAS}$ | Address Setup time | RS | 120 | - | - | ns |
| $t_{SAH}$ | Address Hold time | RS | 80 | - | - | ns |
| $t_{SDS}$ | Data setup time | SID | 160 | -- | - | ns |
| $t_{SDH}$ | Data hold time | SID | 80 | - | - | ns |
| $t_{CSS}$ | CSB Setup Time | CSB | 160 | | | ns |
| $t_{CSH}$ | CSB Hold Time | CSB | 240 | | | ns |

**In 4-SPI Serial Interface (TA = 25℃, VCC = 5V )**

| Symbol | Characteristics | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| *Write Mode (Writing data from MPU to RW1063)* | | | | | | |
| $t_{SCYC}$ | SCLK Cycle Time | SCLK | 480 | - | - | ns |
| $t_w$ | SCLK pulse width | SCLK | 240 | - | - | ns |
| $t_R$,$t_F$ | SCLK Rise/Fall time | SCLK | - | - | 25 | ns |
| $t_{SAS}$ | Address Setup time | RS | 80 | - | - | ns |
| $t_{SAH}$ | Address Hold time | RS | 40 | - | - | ns |
| $t_{SDS}$ | Data setup time | SID | 40 | -- | - | ns |
| $t_{SDH}$ | Data hold time | SID | 40 | - | - | ns |
| $t_{CSS}$ | CSB Setup Time | CSB | 20 | | | ns |
| $t_{CSH}$ | CSB Hold Time | CSB | 160 | | | ns |

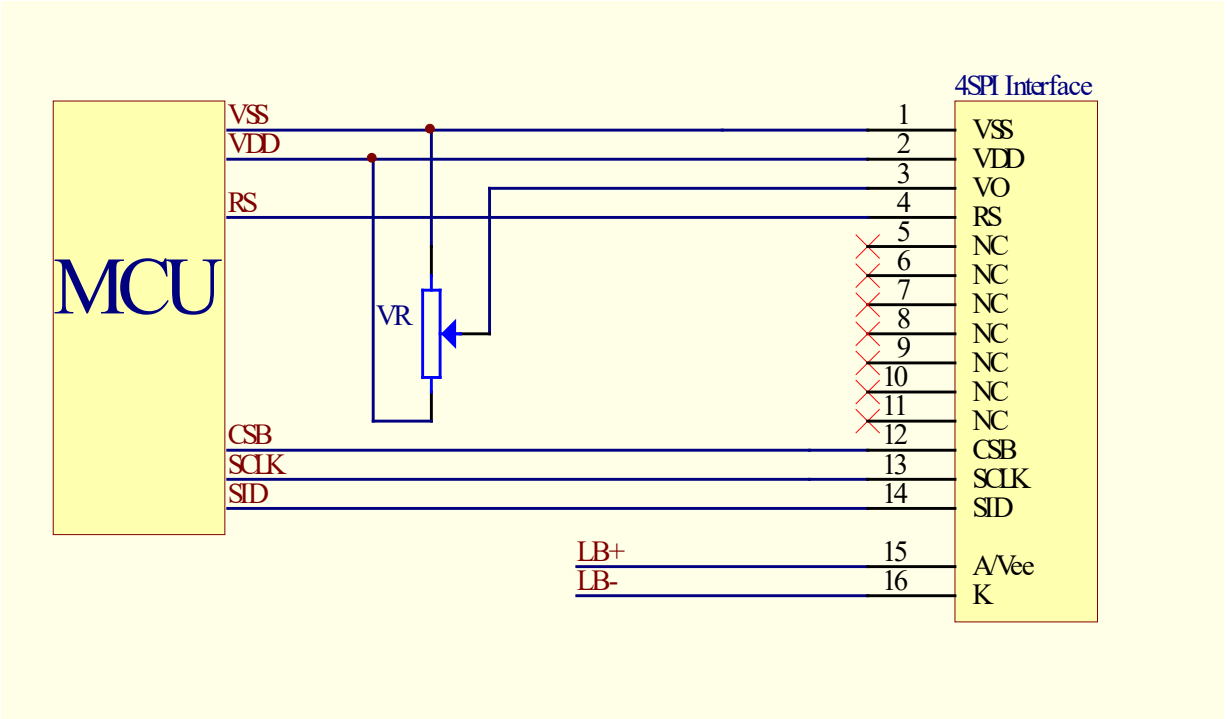
# 4.Initializing of LCM

**Serial Interface Mode(Fosc=540KHz)**



# 5. Recommended circuit diagram

Without negative voltage (Reference)




Build in negative voltage (Reference)

