

MDOG128056AY-BMT	128 x 56	Blue	OLED Module
Specification			
Version: 1		Date: 04/10/2018	
Revision			
1	02/10/2018	First Release.	

Display Features			
Resolution	128 x 56		
Appearance	Blue on Black		
Logic Voltage	2.8V		
Interface	Parallel / SPI / I ² C		
Module Size	42.04 x 63.22 x 1.25 mm		
Operating Temperature	-40°C ~ +70°C		
Construction	COG	Box Quantity	Weight / Display
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* - For full design functionality, please use this specification in conjunction with the SSD1309 specification.(Provided Separately)

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Display Accessories	
Part Number	Description
MDIB-CC1	The MDIB-CC1 is a interconnect board for standard pitch pinouts to fine pitch wires. Ideal for prototyping of TFT and COG LCDs.

Optional Variants	
Appearance	Voltage
White on Black	
Yellow on Black	
Green on Black	



Basic Specifications

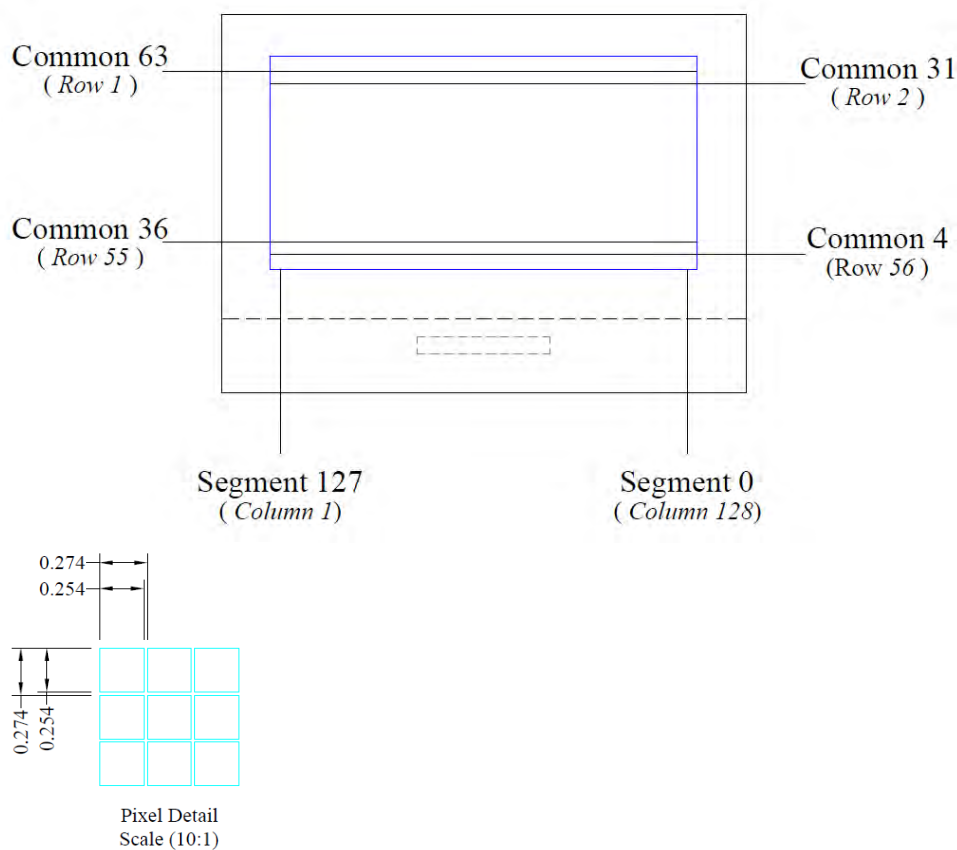
1. Display Specifications

- | | |
|------------------|---------------------------|
| 1) Display Mode | : Passive Matrix |
| 2) Display Color | : Monochrome (Light Blue) |
| 3) Drive Duty | : 1/56 Duty |

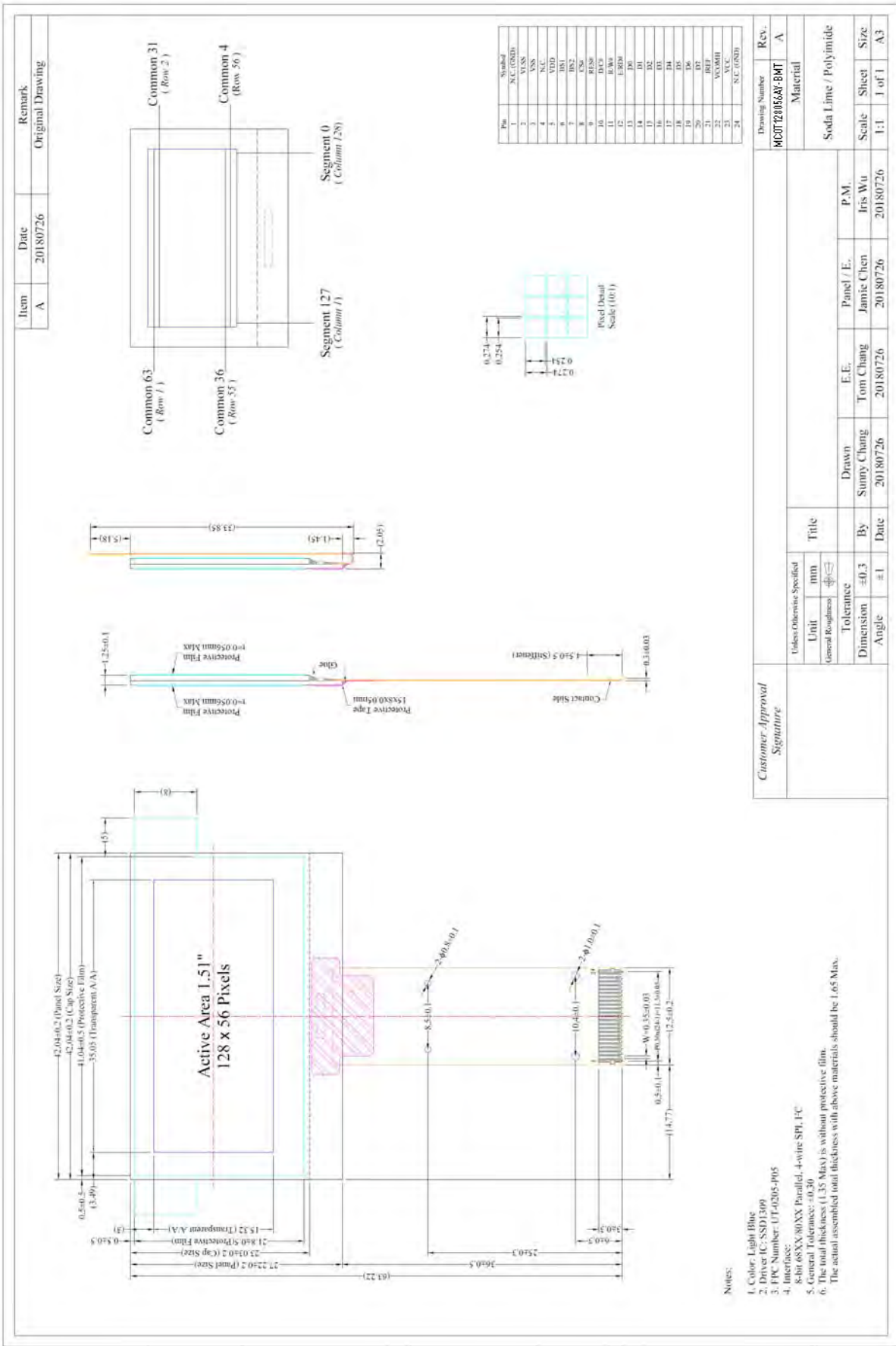
2. Mechanical Specifications

- | | |
|---------------------|--|
| 1) Outline Drawing | : According to the annexed outline drawing |
| 2) Number of Pixels | : 128×56 |
| 3) Module Size | : $42.04 \times 63.22 \times 1.25$ (mm) |
| 4) Panel Size | : $42.04 \times 27.22 \times 1.25$ (mm) |
| 5) Active Area | : 35.05×15.32 (mm) |
| 6) Pixel Pitch | : 0.274×0.274 (mm) |
| 7) Pixel Size | : 0.254×0.254 (mm) |
| 8) Weight | : TBD (g) $\pm 10\%$ |

3. Active Area / Memory Mapping & Pixel Construction



4. Mechanical Drawing



5. Pin Definition

Pin Number	Symbol	I/O	Function															
Power Supply																		
5	VDD	P	Power Supply for Logic Circuit This is a voltage supply pin. It must be connected to external source.															
3	VSS	P	Ground of Logic Circuit This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.															
23	VCC	P	Power Supply for OEL Panel This is the most positive voltage supply pin of the chip. It must be supplied externally.															
2	VLSS	P	Ground of Analog Circuit This is an analog ground pin. It should be connected to V _{SS} externally.															
Driver																		
21	IREF	I	Current Reference for Brightness Adjustment This pin is segment current reference pin. A resistor should be connected between this pin and V _{SS} . Set the current at 10μA maximum.															
22	VCOMH	O	Voltage Output High Level for COM Signal This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and V _{SS} .															
Interface																		
6 7	BS1 BS2	I	Communicating Protocol Select These pins are MCU interface selection input. See the following table: <table><tr><td></td><td>BS1</td><td>BS2</td></tr><tr><td>I²C</td><td>1</td><td>0</td></tr><tr><td>4-wire SPI</td><td>0</td><td>0</td></tr><tr><td>8-bit 68XX Parallel</td><td>0</td><td>1</td></tr><tr><td>8-bit 80XX Parallel</td><td>1</td><td>1</td></tr></table>		BS1	BS2	I ² C	1	0	4-wire SPI	0	0	8-bit 68XX Parallel	0	1	8-bit 80XX Parallel	1	1
	BS1	BS2																
I ² C	1	0																
4-wire SPI	0	0																
8-bit 68XX Parallel	0	1																
8-bit 80XX Parallel	1	1																
9	RES#	I	Power Reset for Controller and Driver This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.															
8	CS#	I	Chip Select This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.															
10	D/C#	I	Data/Command Control This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 will be interpreted as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. When the pin is pulled high and serial interface mode is selected, the data at SDIN will be interpreted as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I ² C mode, this pin acts as SA0 for slave address selection. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.															
12	E/RD#	I	Read/Write Enable or Read This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial or I ² C mode is selected, this pin must be connected to V _{SS} .															
11	R/W#	I	Read/Write Select or Write This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial or I ² C mode is selected, this pin must be connected to V _{SS} .															

5. Pin Definition (Continued)

Pin Number	Symbol	I/O	Function
Interface (Continued)			
13~20	D0~D7	I/O	Host Data Input/Output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I ² C mode is selected, D2, D1 should be tied together and serve as SDA _{OUT} , SDA _{IN} in application and D0 is the serial clock input, SCL. Unused pins must be connected to V _{SS} except for D2 in serial mode.
Reserve			
4	N.C.	-	Reserved Pin The N.C. pin between function pins are reserved for compatible and flexible design.
1, 24	N.C. (GND)	-	Reserved Pin (Supporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.

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Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	4	V	1, 2
Supply Voltage for Display	V_{CC}	0	15	V	1, 2
Operating Temperature	T_{OP}	-40	70	°C	3
Storage Temperature	T_{STG}	-40	85	°C	3
Life Time (120 cd/m ²)		5,000	-	hour	4
Life Time (80 cd/m ²)		12,000	-	hour	
Life Time (60 cd/m ²)		15,000	-	hour	

Note 1: All the above voltages are on the basis of " $V_{SS} = 0V$ ".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: $V_{CC} = 12.5V$, $T_a = 25^{\circ}C$, 50% Checkerboard.

Software configuration follows Section 4.5 Initialization.

End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

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Optics & Electrical Characteristics

1. Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	Note 5	100	120	-	cd/m ²
C.I.E. (Light Blue)	(x) (y)	C.I.E. 1931	0.12 0.22	0.16 0.26	0.20 0.30	
Dark Room Contrast	CR		5000	10000	-	
Viewing Angle			-	Free	-	degree
Transmittance	T	Wavelength 550nm	40	50	-	%

* Optical measurement taken at $V_{DD} = 2.8V$, $V_{CC} = 12.5V$.
Software configuration follows Section 4.5 Initialization.

2. DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}		1.65	2.8	3.3	V
Supply Voltage for Display	V_{CC}	Note 5	12.0	12.5	13.0	V
High Level Input	V_{IH}		$0.8 \times V_{DD}$	-	V_{DD}	V
Low Level Input	V_{IL}		0	-	$0.2 \times V_{DD}$	V
High Level Output	V_{OH}	$I_{OUT} = 100\mu A$, 3.3MHz	$0.9 \times V_{DD}$	-	V_{DD}	V
Low Level Output	V_{OL}	$I_{OUT} = 100\mu A$, 3.3MHz	0	-	$0.1 \times V_{DD}$	V
Operating Current for V_{DD}	I_{DD}		-	180	300	μA
Operating Current for V_{CC}	I_{CC}	Note 6	-	9.5	11.9	mA
		Note 7	-	15.2	19.0	mA
		Note 8	-	27.4	34.3	mA
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	1	5	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	2	10	μA

Note 5: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.

Note 6: $V_{DD} = 2.8V$, $V_{CC} = 12.5V$, 30% Display Area Turn on.

Note 7: $V_{DD} = 2.8V$, $V_{CC} = 12.5V$, 50% Display Area Turn on.

Note 8: $V_{DD} = 2.8V$, $V_{CC} = 12.5V$, 100% Display Area Turn on.

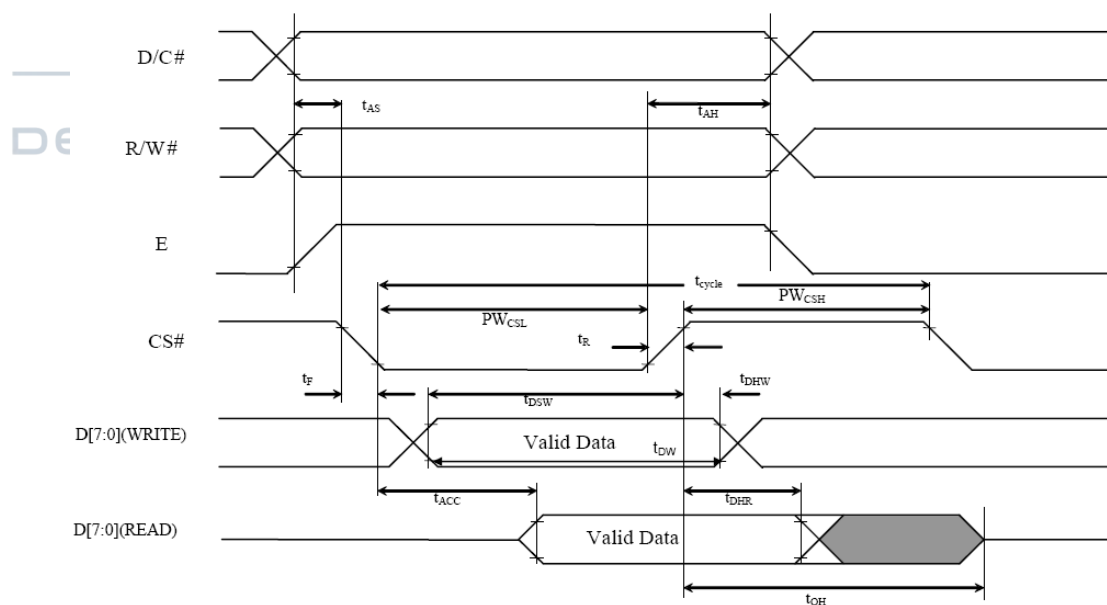
* Software configuration follows Section 4.5 Initialization.

3. AC Characteristics

3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	20	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DW}	Data Write Time	80	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	20	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
t_{R}	Rise Time	-	40	ns
t_{F}	Fall Time	-	40	ns

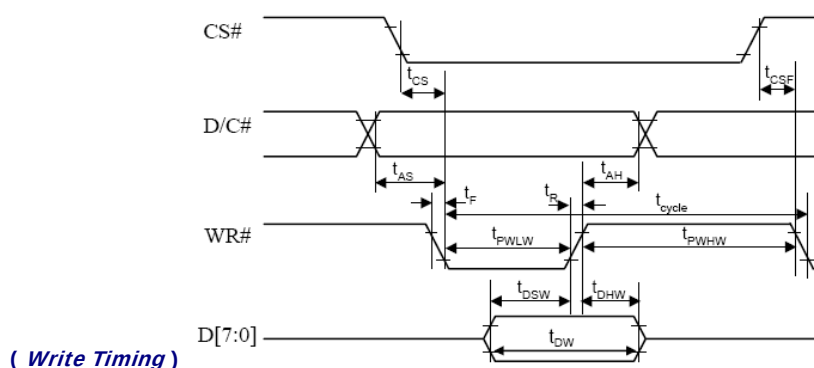
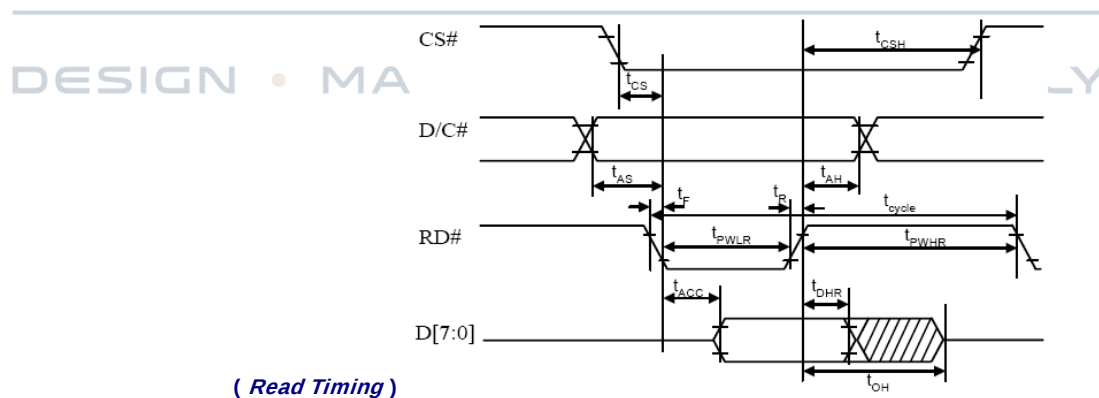
* ($V_{\text{DD}} - V_{\text{SS}} = 1.65\text{V to } 3.3\text{V}$, $T_{\text{a}} = 25^{\circ}\text{C}$)



3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	20	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DW}	Data Write Time	70	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
$t_{\text{PWL R}}$	Read Low Time	120	-	ns
$t_{\text{PWL W}}$	Write Low Time	60	-	ns
$t_{\text{PWH R}}$	Read High Time	60	-	ns
$t_{\text{PWH W}}$	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_{R}	Rise Time	-	40	ns
t_{F}	Fall Time	-	40	ns

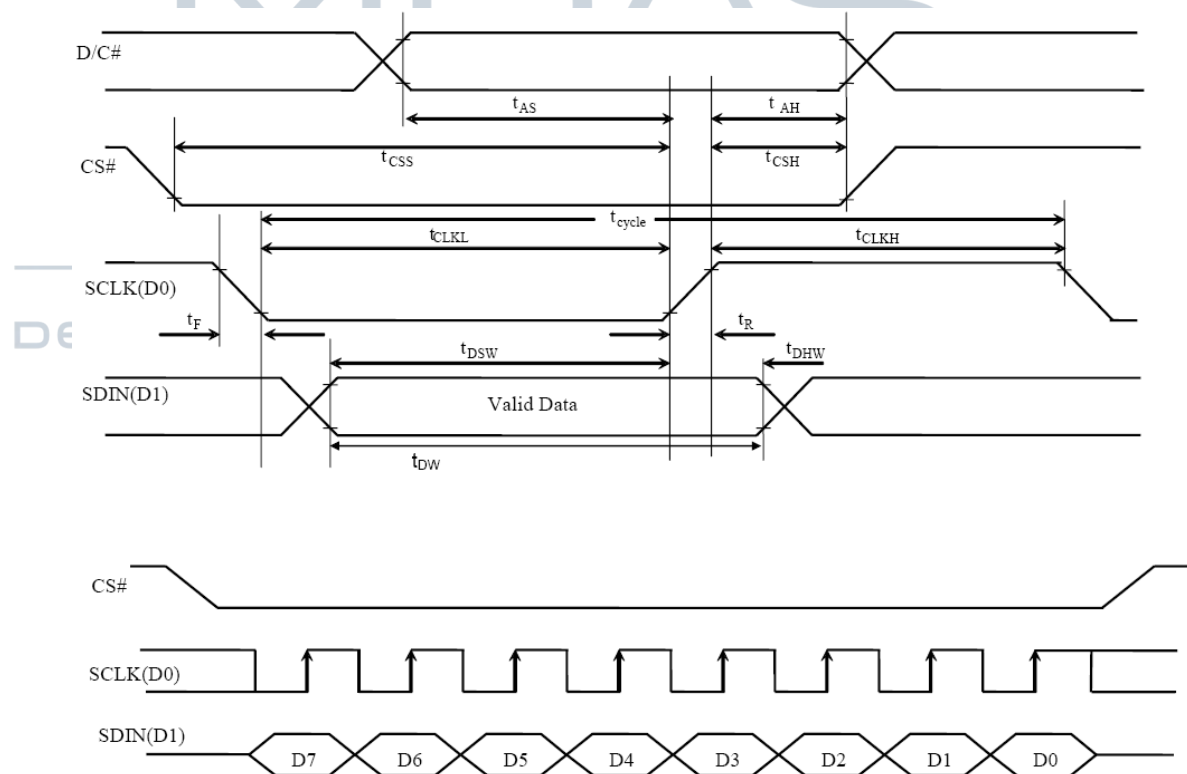
* ($V_{\text{DD}} - V_{\text{SS}} = 1.65\text{V to } 3.5\text{V}$, $T_a = 25^\circ\text{C}$)



3.3 Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	50	-	ns
t_{DW}	Data Write Time	55	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	50	-	ns
t_{CLKH}	Clock High Time	50	-	ns
t_{R}	Rise Time	-	40	ns
t_{F}	Fall Time	-	40	ns

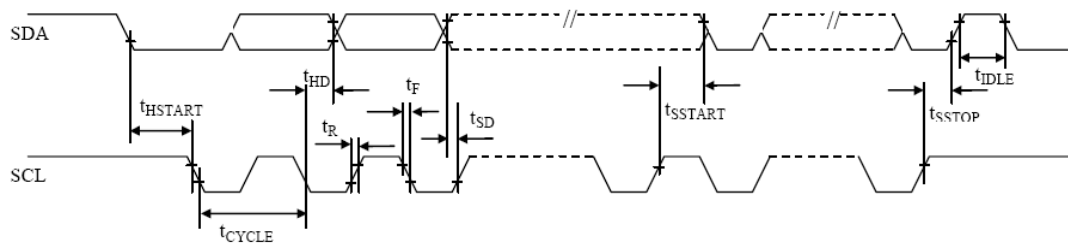
* ($V_{\text{DD}} - V_{\text{SS}} = 1.65\text{V to } 3.5\text{V}$, $T_{\text{a}} = 25^{\circ}\text{C}$)



3.4 I²C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	μs
t_{HSTART}	Start Condition Hold Time	0.6	-	μs
t_{HD}	Data Hold Time (for "SDA _{OUT} " Pin)	0	-	ns
	Data Hold Time (for "SDA _{IN} " Pin)	300		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	μs
t_{SSTOP}	Stop Condition Setup Time	0.6	-	μs
t_{R}	Rise Time for Data and Clock Pin		300	ns
t_{F}	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	μs

* ($V_{\text{DD}} - V_{\text{SS}} = 1.65\text{V to } 3.5\text{V}$, $T_{\text{a}} = 25^{\circ}\text{C}$)



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Functional Specification

1. Commands

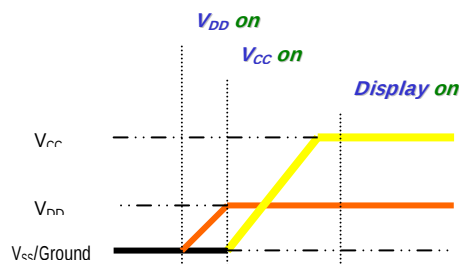
Refer to the Technical Manual for the SSD1309

2. Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

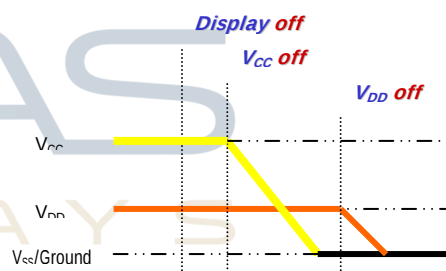
2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
(When V_{CC} is stable)
7. Send Display on command



2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
(When V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



Note 9:

- 1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF.
- 2) V_{CC} should be kept float (disable) when it is OFF.
- 3) Power Pins (V_{DD} , V_{CC}) can never be pulled to ground under any circumstance.
- 4) V_{DD} should not be power down before V_{CC} power down.

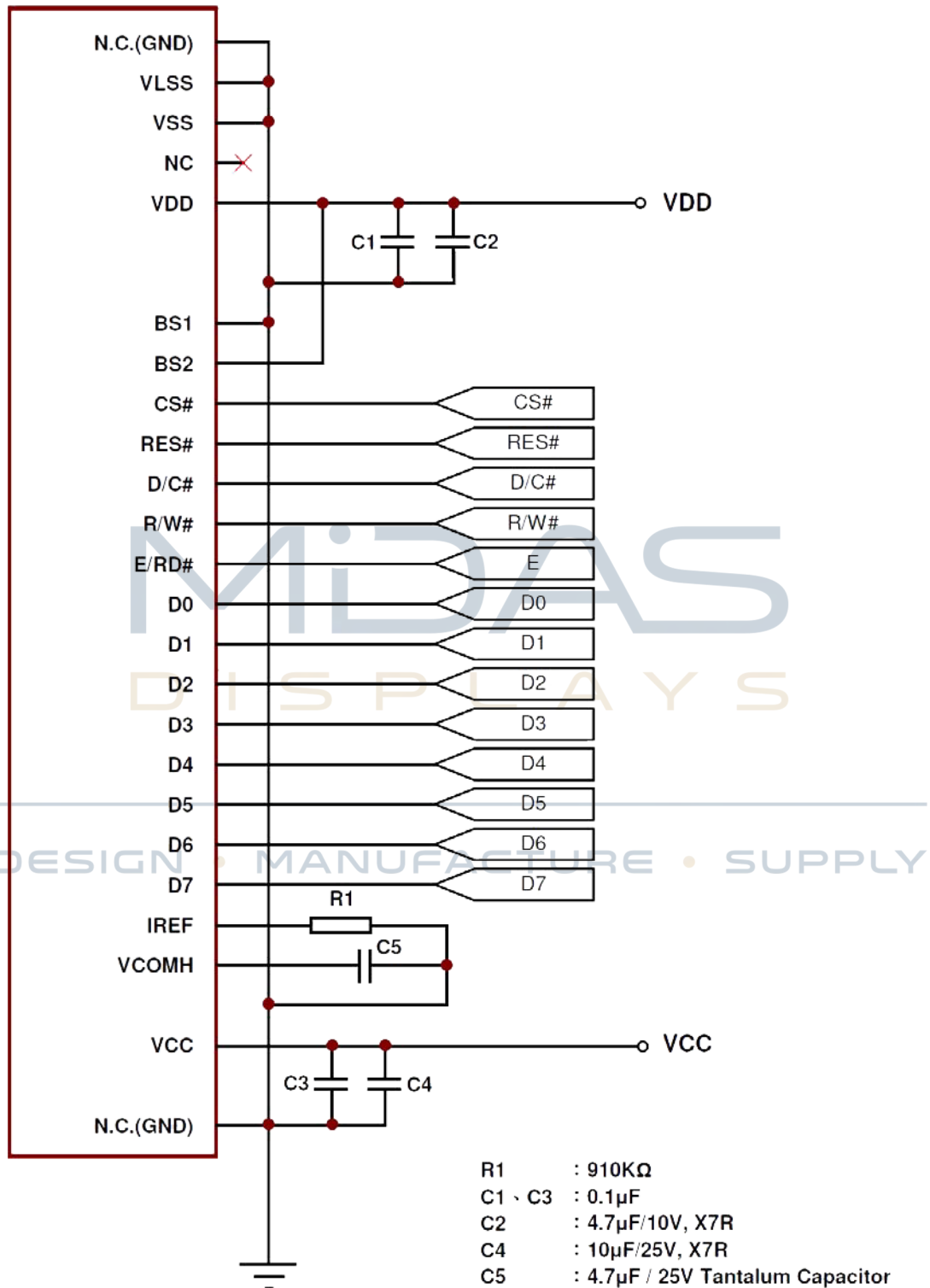
3. Reset Circuit

When RES# input is low, the chip is initialized with the following status:

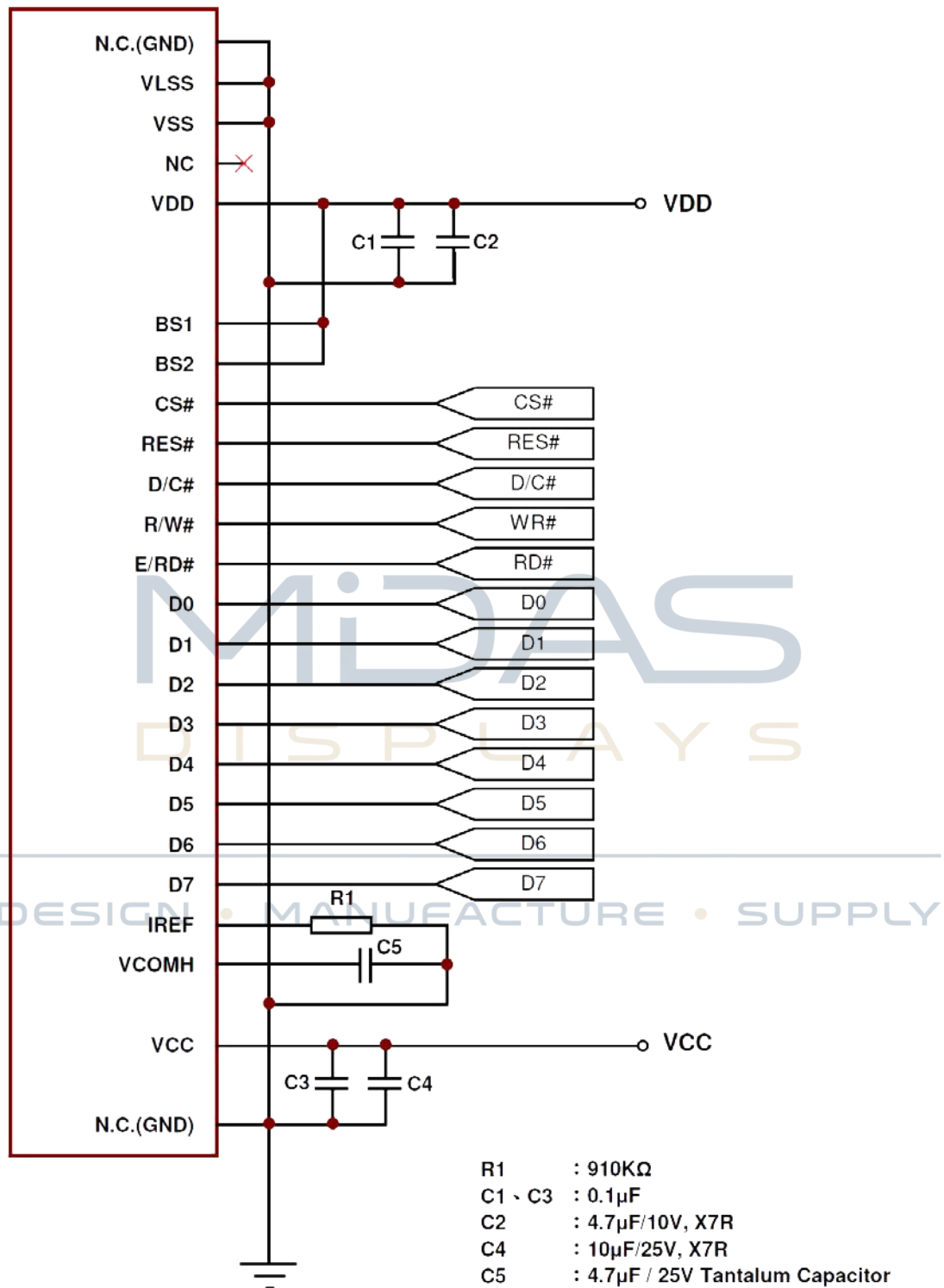
1. Display is OFF
2. 128×64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

4. Application Circuit

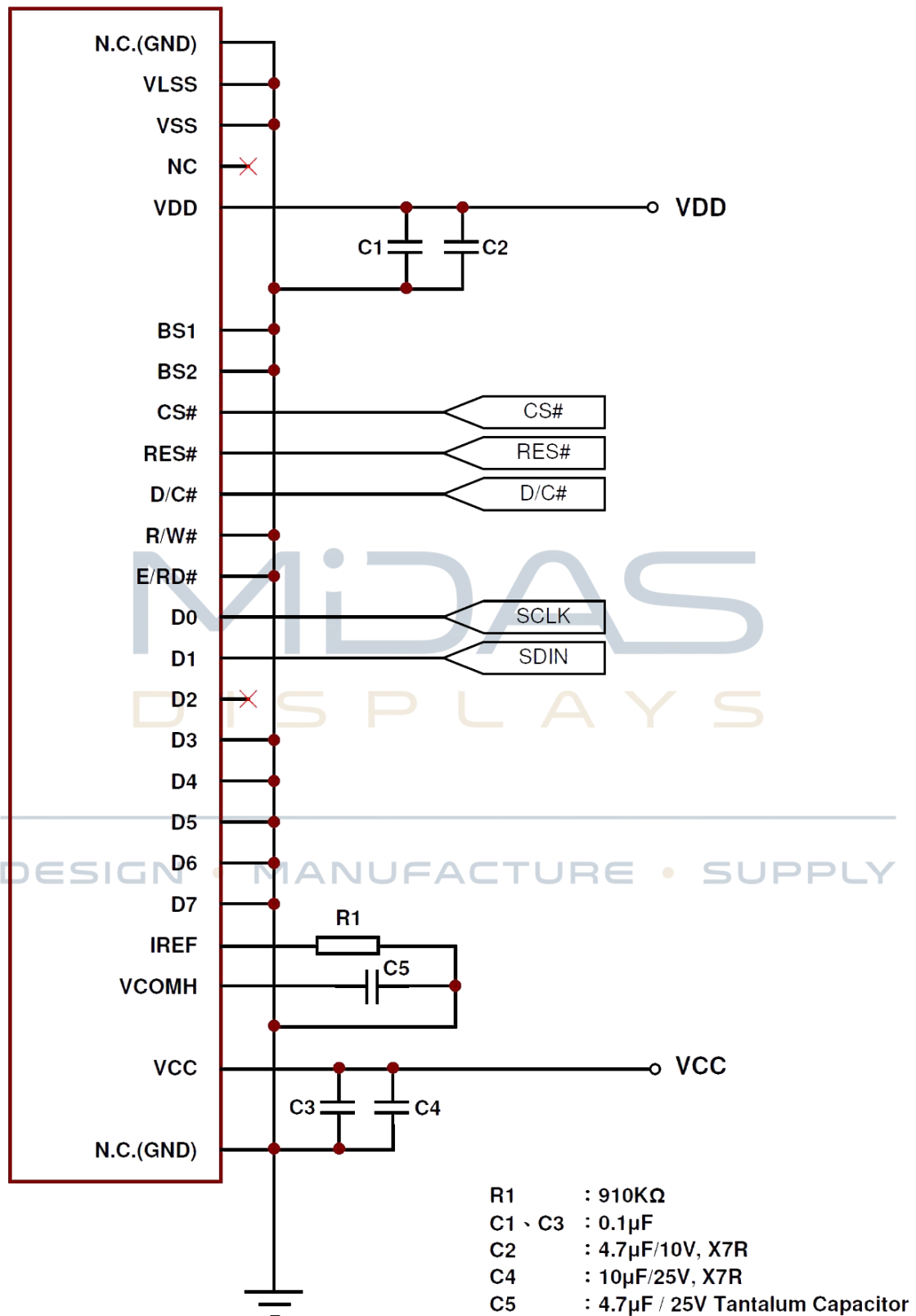
4.1 68xx-Series MPU Parallel Interface



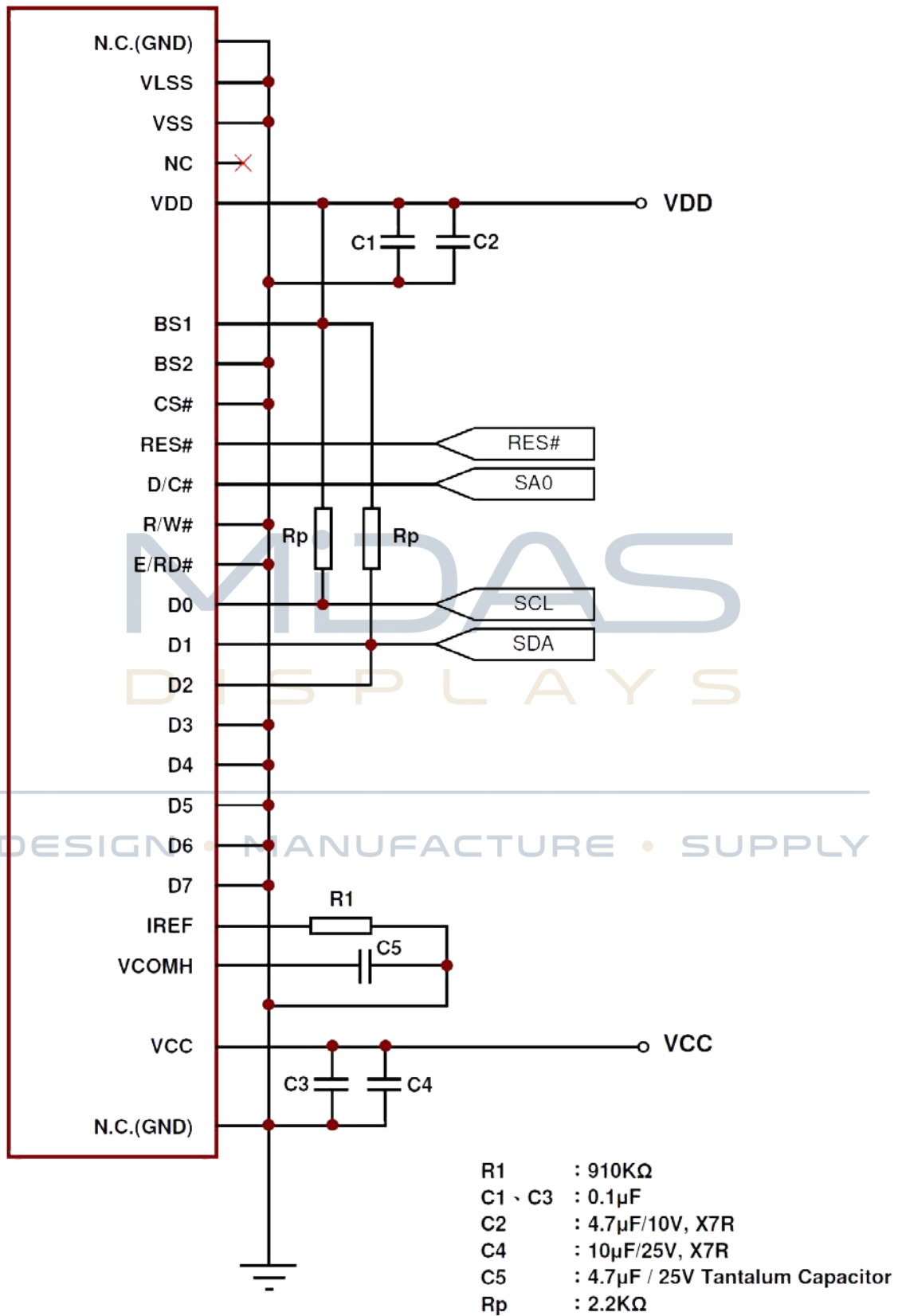
4.2 80xx-Series MPU Parallel Interface



4.3 Serial Interface



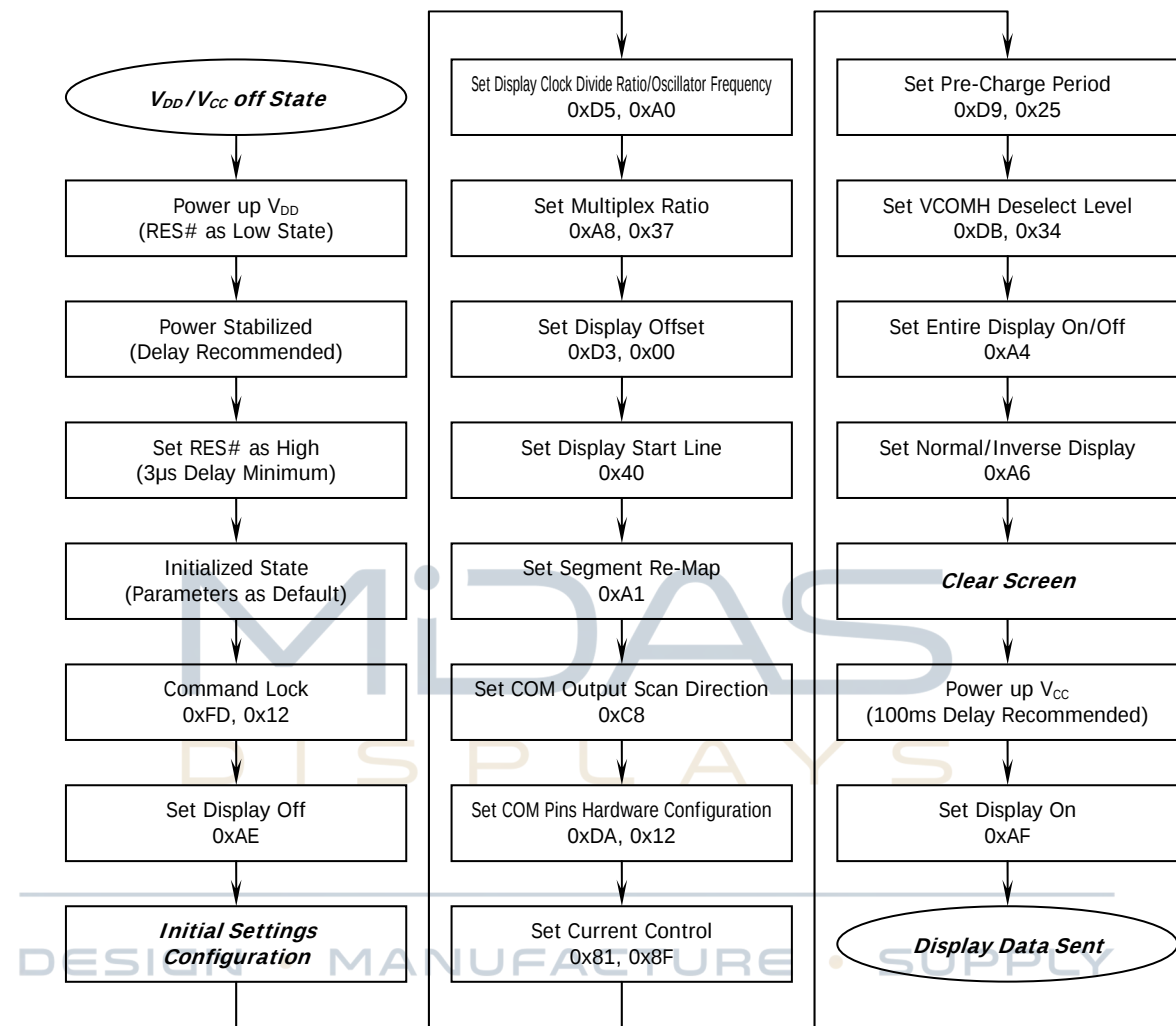
4.4 I²C Interface



5. Actual Application Example

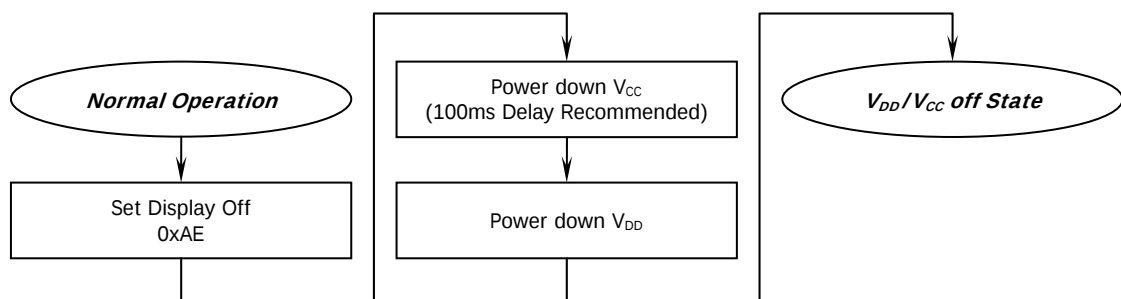
Command usage and explanation of an actual example

<Power up Sequence>

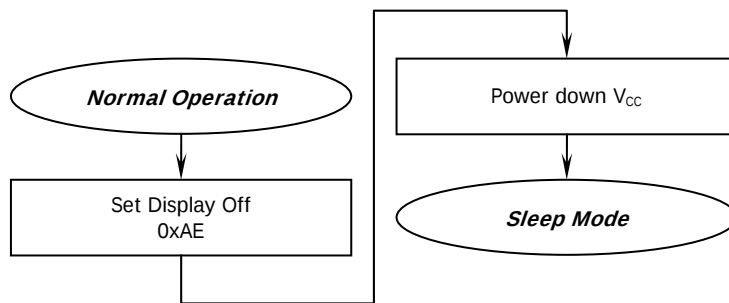


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

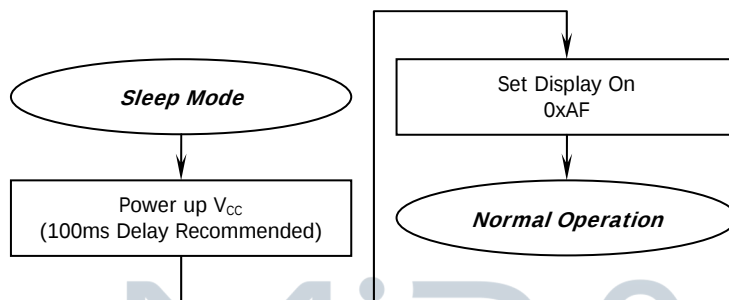
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



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Reliability

1. Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-40°C, 240 hrs	
High Temperature Storage	85°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.

* No moisture condensation is observed during tests.

2. Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

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Outgoing Quality Control Specifications

1. Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	$23 \pm 5^{\circ}\text{C}$
Humidity:	$55 \pm 15\% \text{ RH}$
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	$\geq 50\text{cm}$
Distance between the Panel & Eyes of the Inspector:	$\geq 30\text{cm}$
Finger glove (or finger cover) must be worn by the inspector.	
Inspection table or jig must be anti-electrostatic.	

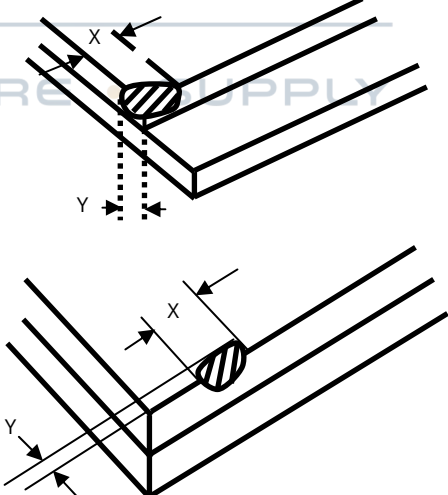
2. Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

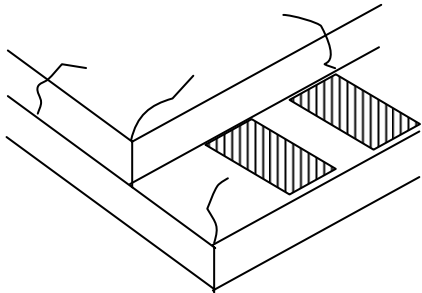
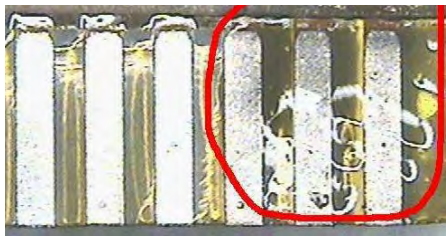
3. Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

3.1 Cosmetic Check (Display Off) in Non-Active Area

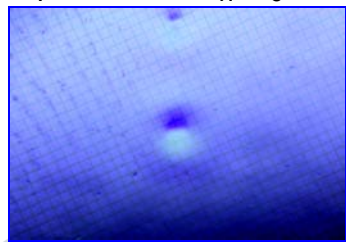
Check Item	Classification	Criteria
Panel General Chipping	Minor	$X > 6 \text{ mm}$ (Along with Edge) $Y > 1 \text{ mm}$ (Perpendicular to edge) 

3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Prober Mark	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

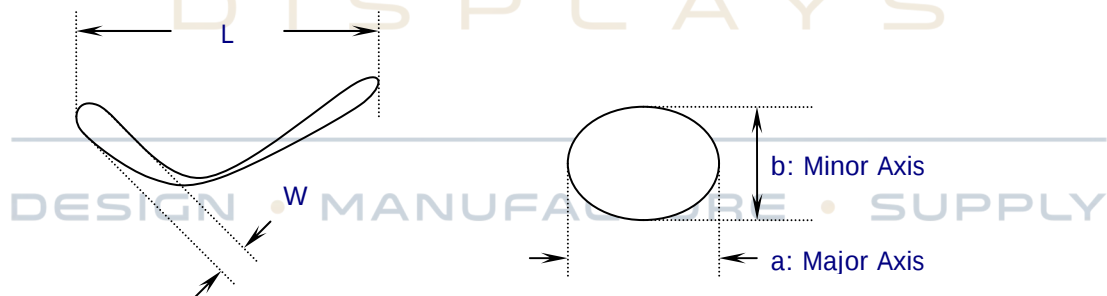
3.2 Cosmetic Check (Display Off) in Active Area

It is recommended to execute in clear room environment (class 10k) if actual in necessary.

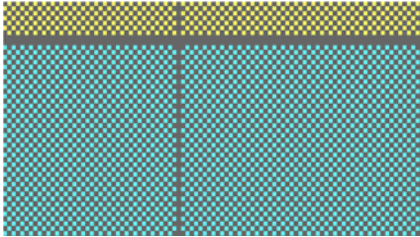
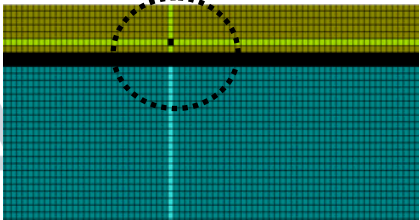
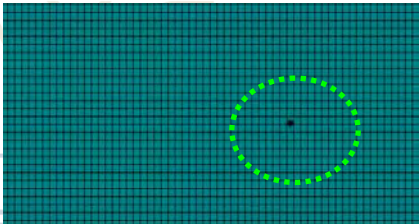
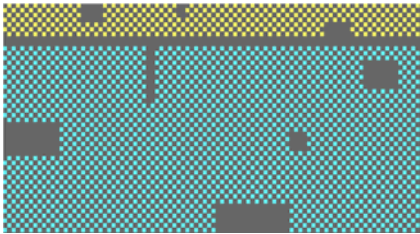
Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	$W \leq 0.1$ Ignore $W > 0.1, L \leq 2$ $n \leq 1$ $L > 2$ $n = 0$
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	$\Phi \leq 0.1$ Ignore $0.1 < \Phi \leq 0.25$ $n \leq 1$ $0.25 < \Phi$ $n = 0$
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	$\Phi \leq 0.5$ → Ignore if no Influence on Display $0.5 < \Phi$ $n = 0$ 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

* Protective film should not be tear off when cosmetic check.

** Definition of W & L & Φ (Unit: mm): $\Phi = (a + b) / 2$



3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	