Sauls Wharf House
Crittens Road
Great Yarmouth
Norfolk
NR31 0AG

Telephone +44 (0)1493 602602
Email:sales@midasdisplays.com
Email:tech@midasdisplays.com
www.midasdisplays.com

MDOT128096AY-WM	128 x 96	White	OLED Module
Specification			
Version: 1		Date: 19/03/2018	
Revision			
1	15/01/2013	First Release.	

Display Features			
Resolution	128 x 96		
Appearance	White on Black		
Logic Voltage	3.3V		
Interface	Parallel / SPI / I²C		
Module Size	32.50 x 36.40 x 1.61 mm		
Operating Temperature	-40°C ~ +70°C	Box Quantity	Weight / Display
Construction	COG	---	---

RoHS compliant

* - For full design functionality, please use this specification in conjunction with the SSD1327 specification.(Provided Separately)

Display Accessories	
Part Number	**Description**

Optional Variants	
Appearance	**Voltage**

CONTENTS

1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by Midas. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

2. WARRANTY

Midas warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). Midas is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, Midas is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Small molecular organic light emitting diode.
- Color : White
- Panel resolution : 128x96
- Driver IC : SSD1327
- Excellent Quick response time : 10μs
- Extremely thin thickness for best mechanism design : 1.61 mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- Strong environmental resistance.
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface, I^2C Interface.
- Wide range of operating temperature : -40 to 70℃
- Anti-glare polarizer.

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 x 96	dot
2	Dot Size	0.19 (W) x 0.19 (H)	mm^2
3	Dot Pitch	0.21 (W) x 0.21 (H)	mm^2
4	Aperture Rate	82	%
5	Active Area	26.86 (W) x 20.14 (H)	mm^2
6	Panel Size	32.5 (W) x 29.2 (H)	mm^2
7*	Panel Thickness	1.42 ± 0.1	mm
8	Module Size	32.5 (W) x 36.4 (H) x 1.61 (T)	mm^3
9	Diagonal A/A size	1.32	inch
10	Module Weight	3.1 ± 10%	gram

* Panel thickness includes substrate glass, cover glass and UV glue thickness.

5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{CI})	-0.3	4	V	Ta = 25℃	IC maximum rating
Supply Voltage (Vcc)	8	19	V	Ta = 25℃	IC maximum rating
Operating Temp.	-40	70	℃		
Storage Temp	-40	85	℃		
Humidity		85	%		
Life Time	13,000	-	Hrs	100 cd/m^2, 50% checkerboard	Note (1)
Life Time	16,000	-	Hrs	80 cd/m^2, 50% checkerboard	Note (2)

Note:

(A) Under Vcc = 15V, Ta = 25℃, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 100 cd/m^2 :

- Contrast setting : 0x5f
- Frame rate : 105Hz
- Duty setting : 1/96

(2) Setting of 80 cd/m^2 :

- Contrast setting : 0x4f
- Frame rate : 105Hz
- Duty setting : 1/96

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Driver power supply (for OLED panel)	-	14.5	15	15.5	V
V_{CI}	Low voltage power supply	-	2.6	-	3.5	V
V_{OH}	High logic output level	Iout=100 uA,	0.9* V_{CI}	-	V_{CI}	V
V_{OL}	Low logic output level	Iout=100uA,	0	-	0.1* V_{CI}	V
V_{IH}	High logic input level	Iout=100uA,	0.8* V_{CI}	-	V_{CI}	V
V_{IL}	Low logic input level	Iout=100uA,	0	-	0.2* V_{CI}	V
I_{CC}	V_{CC} Supply Current	V_{CI} = 3.5V, V_{CC} = 18V, Display ON, No panel attached, contrast = FF	External V_{DD}= 2.5V	600	750	uA
			Internal V_{DD}= 2.5V	600	750	
I_{CI}	V_{CI} Supply Current	V_{CI} = 3.5V, V_{CC} = 18V, Display ON, No panel attached, contrast = FF	External V_{DD}= 2.5V	35	50	uA
			Internal V_{DD}= 2.5V	95	120	
I_{SEG}	Segment output current Setting V_{CC}=18V, IREF=10uA	Contrast=FF	-	300	370	uA
		Contrast=AF	-	206	-	uA
		Contrast=7F	-	150	-	uA
		Contrast=3F	-	75	-	uA
		Contrast=1F	-	37.5	-	uA

6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current consumption	-	25.5	27.5	mA	All pixels on
Standby mode current consumption	-	1	2	mA	Standby mode 10% pixels on
Normal mode power consumption	-	382.5	412.5	mW	All pixels on
Standby mode power consumption	-	15	30	mW	Standby mode 10% pixels on
Pixel Luminance	80	100		cd/m^2	Display Average
Standby Luminance		10		cd/m^2	
CIEx (White)	0.24	0.28	0.32		CIE1931
CIEy (White)	0.28	0.32	0.36		CIE1931
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		µs	

Normal mode condition :

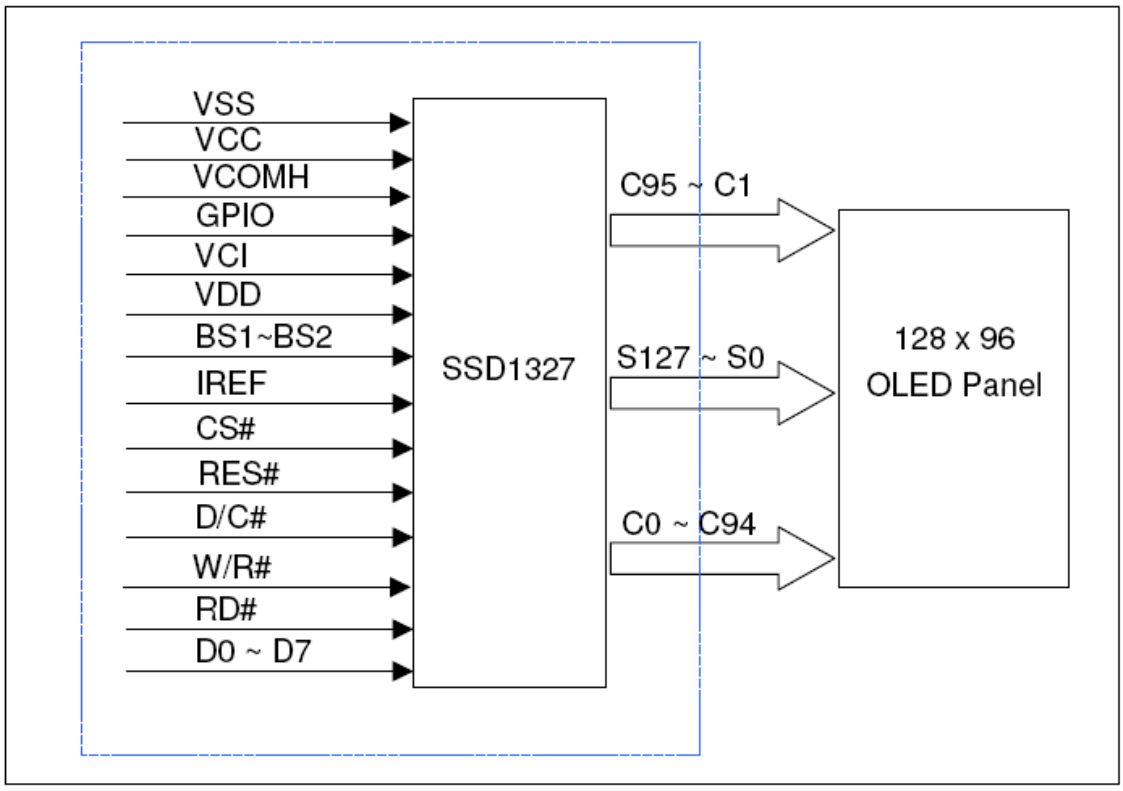
- Driving Voltage : 15V
- Contrast setting : 0x5f
- Frame rate : 105Hz
- Duty setting : 1/96

Standby mode condition :

- Driving Voltage : 15V
- Contrast setting : 0x0a
- Frame rate : 105Hz
- Duty setting : 1/96

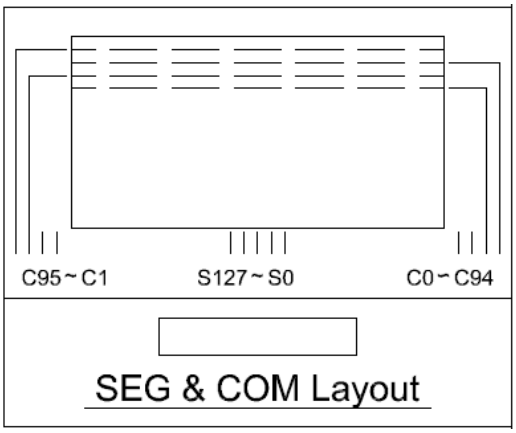
7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



Midas 128x96 OLED Module

7.2 PANEL LAYOUT DIAGRAM



7.3 PIN ASSIGNMENTS

PIN NAME	PIN NO	DESCRIPTION
VSS	1	Ground.
VCC	2	Power supply for analog circuit.
VCOMH	3	Com Voltage Output. A capacitor should be connected between this pin and V_{SS}.
GPIO	4	General I/O port.
VCI	5	Power supply for logic circuit.
VDD	6	A capacitor should be connected between this pin and V_{SS}.
BS1	7	Interface selection input.
BS2	8	
VSS	9	Ground.
IREF	10	Reference current input pin. A resistor should be connected between this pin and V_{SS}.
CS#	11	Chip select input.
RES#	12	Reset signal input. When it's low, initialization of SSD1327 is executed.
D/C	13	Data/ Command control. Pull high for write/read display data. Pull low for write command or read status.
WR#	14	This pin is used to receive the write data signal.
RD#	15	This pin is used to receive the read data signal.
D0	16	Data bus (for parallel interface)
D1	17	
D2	18	
D3	19	
D4	20	
D5	21	
D6	22	
D7	23	
VCC	24	Power supply for analog circuit.
VSS	25	Ground.

7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x128x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. The GDDRAM address maps below tables show some examples on using the command “Set Re-map” A0h to re-map the GDDRAM. In the following tables, the lower nibble and higher nibble of D0, D1, D2 … D8189, D8190, D8191 represent the 128x128 data bytes in the GDDRAM.

The GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
  Disable Column Address Re-map (A[0]=0)
  Disable Nibble Re-map (A[1]=0)
  Enable Horizontal Address Increment (A[2]=0)
  Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D8191

GDDRAM address map 1

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	(HEX)
COM1	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
|	|									
COM126	7E	D8064[3:0]	D8064[7:4]	D8065[3:0]	D8065[7:4]		D8126[3:0]	D8126[7:4]	D8127[3:0]	D8127[7:4]	
COM127	7F	D8128[3:0]	D8128[7:4]	D8129[3:0]	D8129[7:4]		D8190[3:0]	D8190[7:4]	D8191[3:0]	D8191[7:4]	
COM Outputs	Row Address (HEX)										

Nibble re-map A[1]=0

The GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Vertical Address Increment (A[2]=1)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D8191

GDDRAM address map 2

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM0	00	D0[3:0]	D0[7:4]	D128[3:0]	D128[7:4]		D7936[3:0]	D7936[7:4]	D8064[3:0]	D8064[7:4]
COM1	01	D1[3:0]	D1[7:4]	D129[3:0]	D129[7:4]		D7937[3:0]	D7937[7:4]	D8065[3:0]	D8065[7:4]
|	|									
COM126	7E	D126[3:0]	D126[7:4]	D254[3:0]	D254[7:4]		D8062[3:0]	D8062[7:4]	D8190[3:0]	D8190[7:4]
COM127	7F	D127[3:0]	D127[7:4]	D255[3:0]	D255[7:4]		D8063[3:0]	D8063[7:4]	D8191[3:0]	D8191[7:4]

SEG Outputs Column Address (HEX)

COM Outputs

Row Address (HEX)

(Display Startline=0)

Nibble re-map A[1]=0

The GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
  - Enable Column Address Re-map (A[0]=1)
  - Enable Nibble Re-map (A[1]=1)
  - Enable Horizontal Address Increment (A[2]=0)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D8191

GDDRAM address map 3

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		3F		3E			01		00	
COM0	00	D63[7:4]	D63[3:0]	D62[7:4]	D62[3:0]		D1[7:4]	D1[3:0]	D0[7:4]	D0[3:0]
COM1	01	D127[7:4]	D127[3:0]	D126[7:4]	D126[3:0]		D65[7:4]	D65[3:0]	D64[7:4]	D64[3:0]
|	|									
COM126	7E	D8127[7:4]	D8127[3:0]	D8126[7:4]	D8126[3:0]		D8065[7:4]	D8065[3:0]	D8064[7:4]	D8064[3:0]
COM127	7F	D8191[7:4]	D8191[3:0]	D8190[7:4]	D8190[3:0]		D8129[7:4]	D8129[3:0]	D8128[7:4]	D8128[3:0]

SEG Outputs Column Address (HEX)

COM Outputs

Row Address (HEX)

(Display Startline=0)

Nibble re-map A[1]=1

The example in which the display start line register is set to 10h with the following condition:

- Command “Set Re-map” A0h is set to:
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Horizontal Address Increment (A[2]=0)
  - Enable COM Re-map (A[4]=1)
- Display Start Line=78h (corresponds to COM119)
- Data byte sequence: D0, D1, D2 … D8191

GDDRAM address map 4

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM119	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]
COM118	01	D1[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]
|	|								
COM121	7E	D126[3:0]	D8064[7:4]	D8065[3:0]	D8065[7:4]		D8126[3:0]	D8126[7:4]	D8127[3:0]	D8127[7:4]
COM120	7F	D127[3:0]	D8128[7:4]	D8129[3:0]	D8129[7:4]		D8190[3:0]	D8190[7:4]	D8191[3:0]	D8191[7:4]

SEG Outputs Column Address (HEX)

COM Outputs / Row Address (HEX)

(Display Startline=78H)

Nibble re-map A[1]=0

The GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Horizontal Address Increment (A[2]=0)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Column Start Address=01h
- Column End Address=3Eh
- Row Start Address=01h
- Row End Address=7Eh
- Data byte sequence: D0, D1, D2 … D7811

GDDRAM address map 5

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM0	00									
COM1	01			D0[3:0]	D0[7:4]		D61[3:0]	D61[7:4]		
|	|								
COM126	7E			D7750[3:0]	D7750[7:4]		D7811[3:0]	D7811[7:4]		
COM127	7F									

SEG Outputs Column Address (HEX)

COM Outputs / Row Address (HEX)

(Display Startline=0)

Nibble re-map A[1]=0

7.5 INTERFACE TIMING CHART

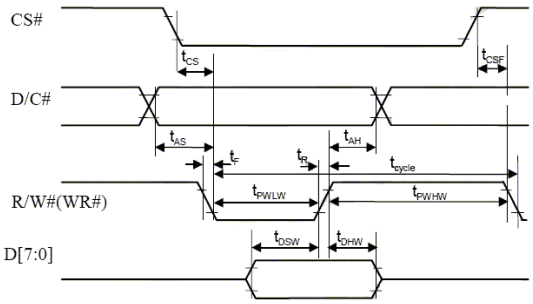
8080-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{CI} = 3.3V, T_A = 25°C)

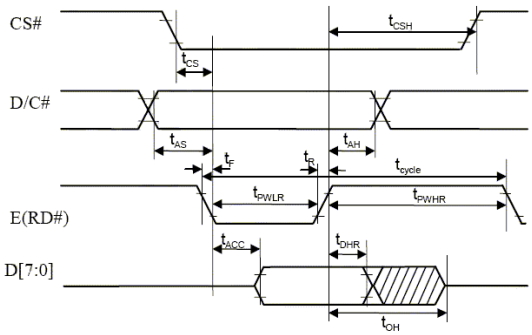
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series MCU parallel interface characteristics

Write cycle



Read cycle



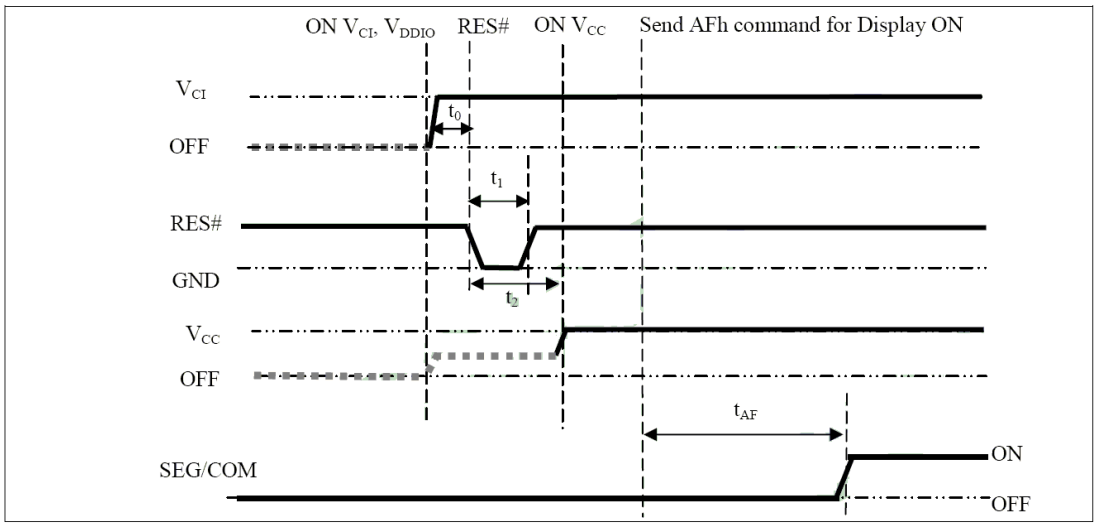
8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE

Power ON sequence:

1. Power ON V_{CI}.
2. After V_{CI} becomes stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 100us (t_1) [4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON V_{CC}.[1]
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).

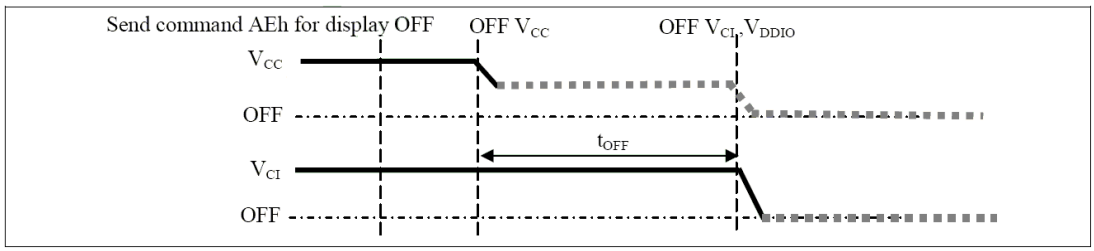
The Power ON sequence.



***Power OFF sequence*:**

1. Send command AEh for display OFF.
2. Power OFF V_{CC}.[1], [2], [3]
3. Wait for t_{OFF}. Power OFF V_{CI}.(where Minimum t_{OFF}=80ms [5], Typical t_{OFF}=100ms)

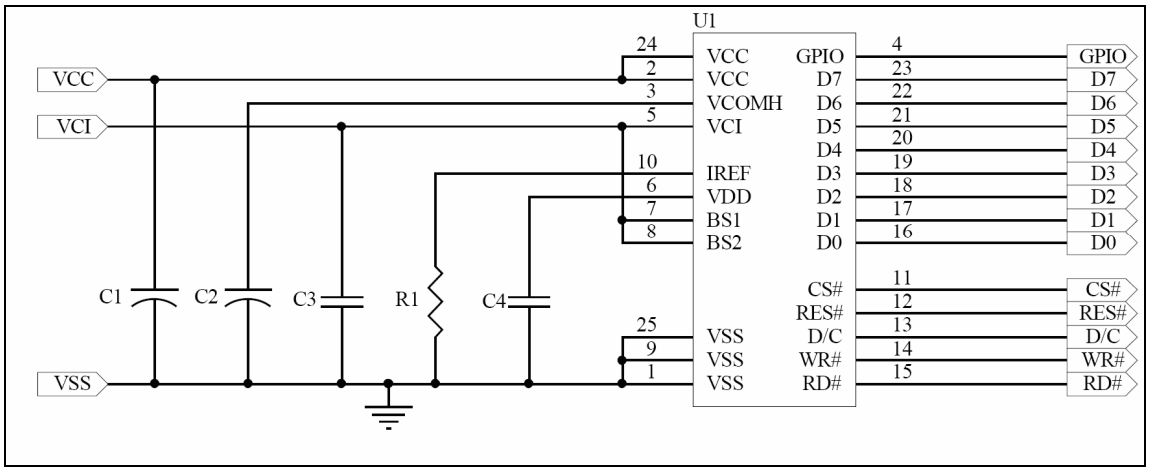
The Power OFF sequence



Note:

(1) Since an ESD protection circuit is connected between V_{CI} and V_{CC}, V_{CC} becomes lower than V_{CI} whenever V_{CI} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.
(2) V_{CC} should be kept disable when it is OFF.
(3) Power pins (V_{CI}, V_{CC}) can never be pulled to ground under any circumstance.
(4) The register values are reset after t_1.
(5) V_{CI} should not be Power OFF before V_{CC} Power OFF

8.2 APPLICATION CIRCUIT



Component:

C1, C2: 4.7uF/35V(Tantalum type) or VISHAY (572D475X0025A2T)

C3, C4: 1uF/16V(0603)

R1: 1M ohm (0603) 1%

This circuit is for 8080 8bits interface.

8.3 COMMAND TABLE

Refer to IC Spec.: SSD1327

9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85℃, 240hrs	5
2	High temp. (Operation)	70℃, 120hrs	5
3	Low temp. (Operation)	-40℃, 120hrs	5
4	High temp. / High humidity (Operation)	65℃, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40℃ ~85℃ (-40℃ /30min; transit /3min; 85℃ /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

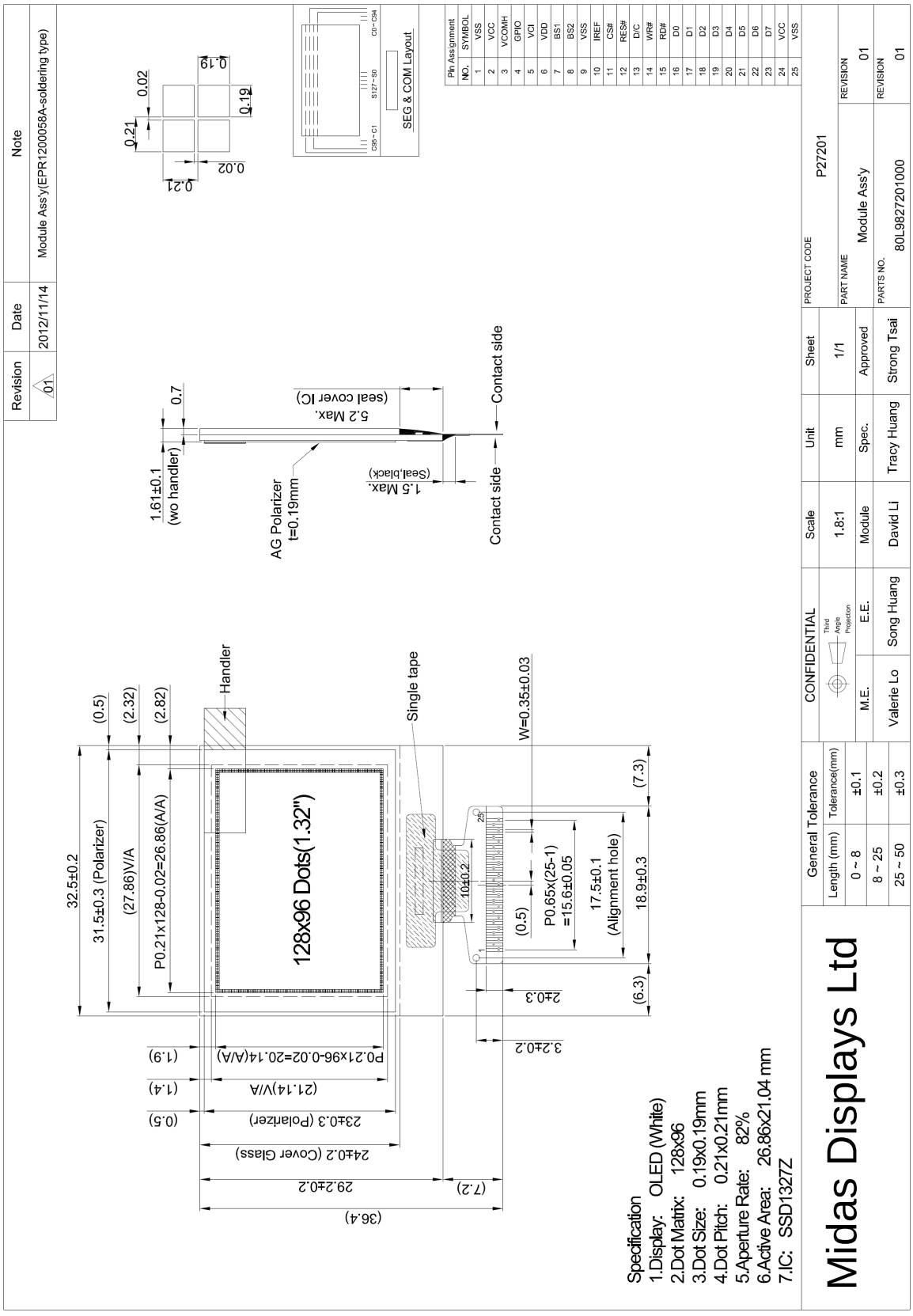
Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

10. EXTERNAL DIMENSION



12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

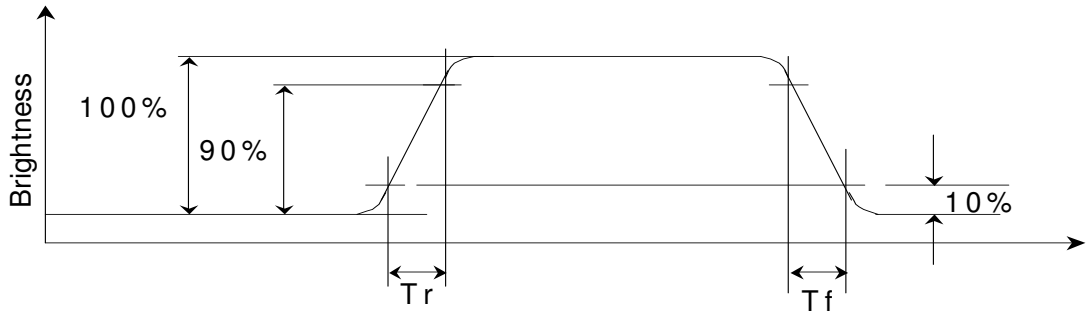


Figure 2 Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

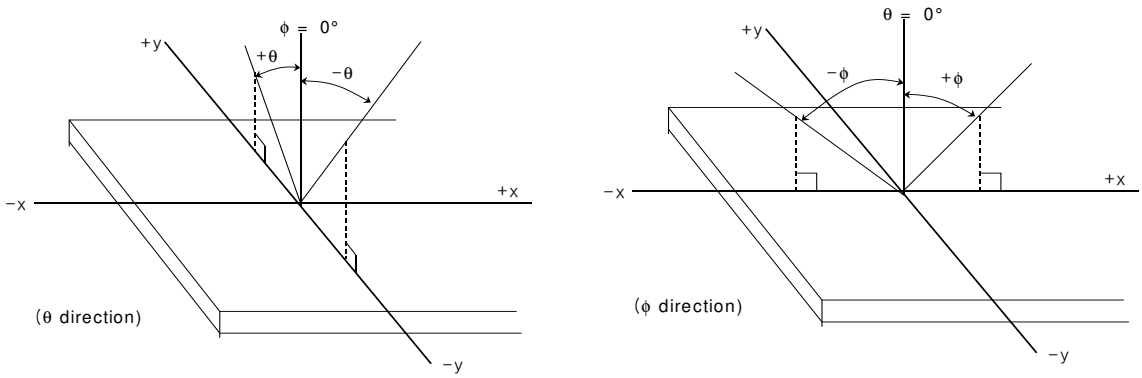
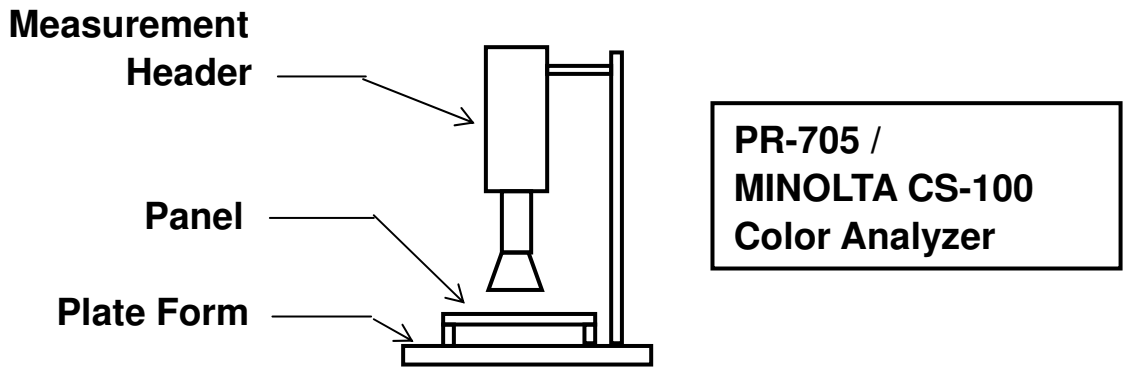


Figure 3 Viewing angle

APPENDIX 2: MEASUREMENT APPARATUS

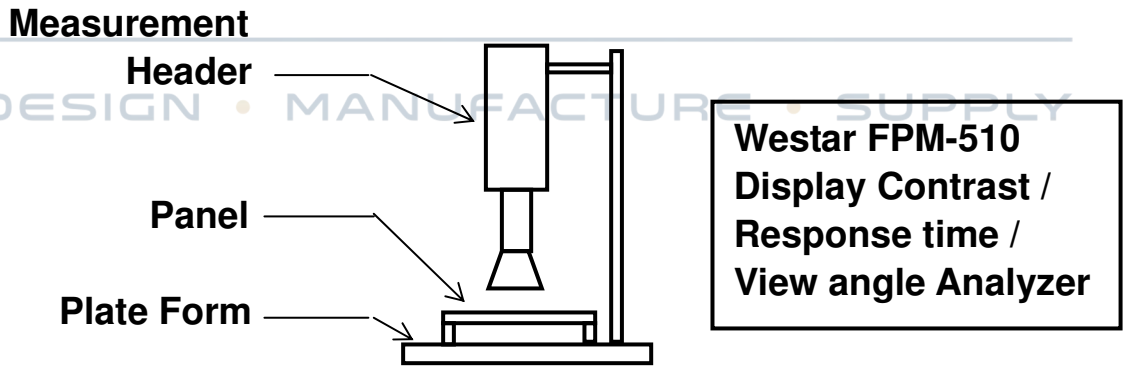
A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100

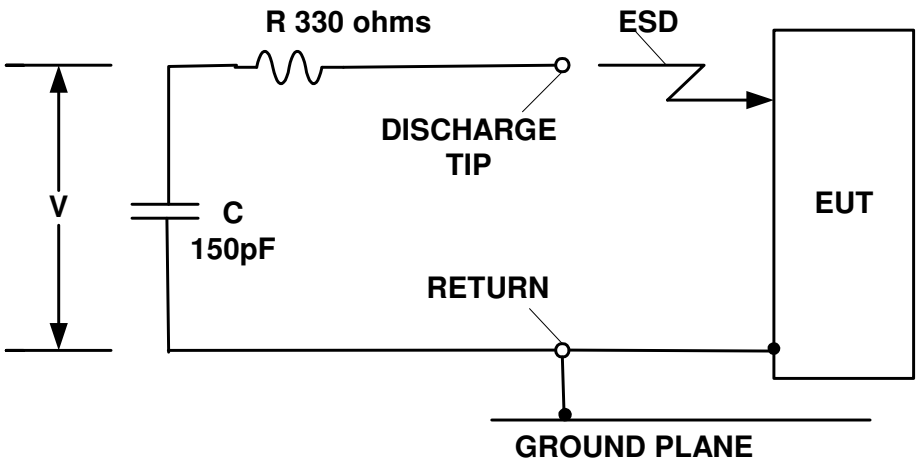


B. CONTRAST / RESPONSE TIME / VIEWING ANGLE

WESTAR CORPORATION FPM-510



C. ESD ON AIR DISCHARGE MODE



APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.