

MDT156003	1920 x 1080	LVDS Interface	TFT Module
Specification			
Version: 1		Date: 21/04/2022	
Revision			
1	19/04/2022	First issue	

Display Features			
Display Size	15.6"		
Resolution	1920 x 1080		
Orientation	Landscape		
Appearance	RGB		
Logic Voltage	3.3V		
Interface	LVDS		
Brightness	2000 cd/m ²		
Touchscreen	---		
Module Size	363.8 x 215.9 x 8.8 mm		
Operating Temperature	-30°C ~ +85°C	Created By	Checked By
Pinout	40 way FFC	RV	TSB
Pitch	0.5 mm	Box Quantity	Weight / Display
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Display Accessories	
Part Number	Description
MBID-40FP	40 Way FFC to cable and wires. Driven by any driver board that can be wired to a 1mm pitch SHDR-40V-S-B receptacle.
MDIB-CC1	Interconnect board for standard pitch pinouts to fine pitch wires. Providing pinouts for 2.54 pinout. 1.27, 1, 0.845, 0.8, 0.7, 0.65, 0.62, 0.6, 0.5 & 0.3 pads.

Optional Variants	
Appearances	Voltage



1. HANDLING PRECAUTIONS

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open or modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 10) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentarily. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

2. General Description

2.1, Overview

MDT156003 module is a color active matrix LCD module incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver ICs, control circuit, power supply circuit and a White-LED Backlight unit. Graphics and texts can be displayed on a 1920×RGB×1080 dots panel with about 16.7M colors (RGB 8-bits data driver). All input signals are LVDS interface compatible. The BLU driving current source for backlight LED driving by external LED driver.

2.2 Features

- High brightness display, 2000nits by LED backlight.
- Hi-tni LC applied
- 100K Hrs extra Long operation lifetime BLU design
- 72% NTSC (typ.)
- RoHS Compliance
- With low power density solution



2.4 Display Specifications

Items	Unit	Specification
Screen Diagonal	mm	15.6 inch
Active Area	mm	344.16(H) X 193.59(V)
Pixels H x V	pixels	1920 x3(RGB) x 1080
Pixels Pitch	um	179.25 (per one triad) x 179.25
Pixel Arrangement		RGB Vertical stripe
Display mode		Normally black
White luminance (center)	Cd/m ²	2000 (Typ.)
Contrast ratio		800:1 (Typ.)
Optical Response Time	msec	25 ms (Typ. on/off)
Normal Input Voltage VDD	Volt	3.3
Power Consumption (Vcc Line + LED backlight)	Watt	27.4 W (VDD line=4 W; LED lines= 23.4 W)
Weight	Grams	1055
Physical size	mm	363.8(W)×215.9(H)×8.8(D, max)
Electrical Interface		2 channel LVDS
Support Colors		16.7M colors (RGB 8-bit + FRC)
Surface Treatment		Anti-glare and hard-coating 3H
Temperature range		
Operating	°C	-30 ~ 85 (TFT surface)
Storage	°C	-40 ~ 90
RoHS Compliance		RoHS Compliance



2.5 Optical Characteristics

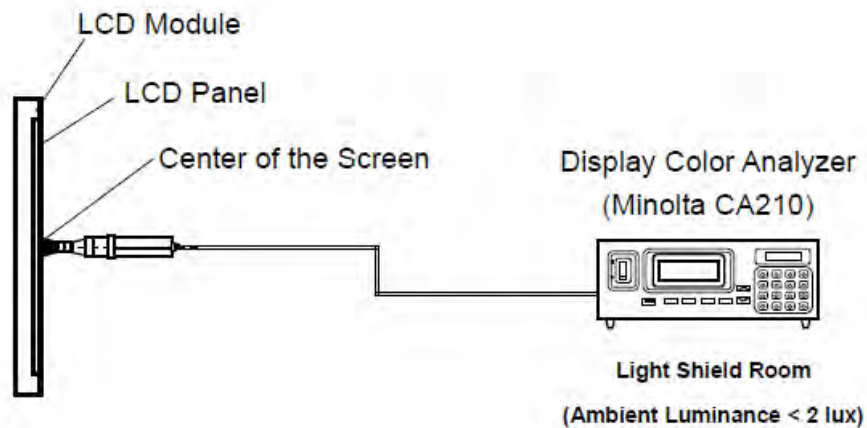
The following optical characteristics are measured under stable condition at 25 °C

Items	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing angle	Deg.	Horizontal (Right)	80	89		2
		CR=10 (Left)	80	89		
		Vertical (Up)	80	89		
		CR=10 (Down)	80	89		
Contrast Ratio		Normal Direction	600	800		3
Response Time	msec	Raising time (T_{rR})		13		4
		Falling time (T_{rF})		12		
		Raising + Falling		25	35	
Color / Chromaticity Coordinates (CIE)		Red x	-0.05	0.652	+0.05	5
		Red y		0.338		
		Green x		0.333		
		Green y		0.613		
		Blue x		0.150		
		Blue y		0.050		
Color coordinates (CIE) White		White x		0.313		
		White y		0.329		
Center Luminance	Cd/m ²		1600	2000		6
Luminance Uniformity	%		70	75		7
NTSC	%			72		

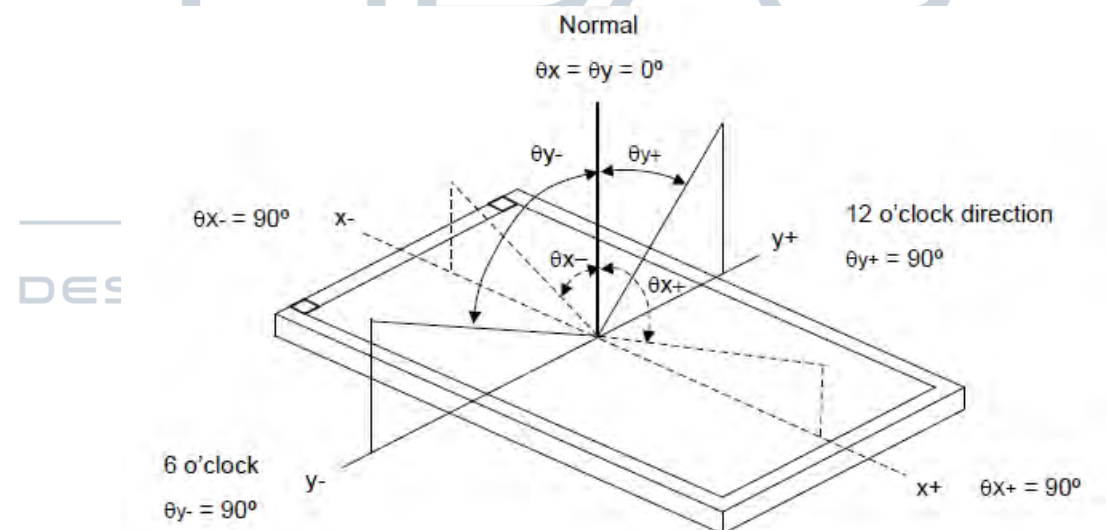


Note 1: Measurement method

The LCD module should be stabilized at given temperature for 0.5 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.



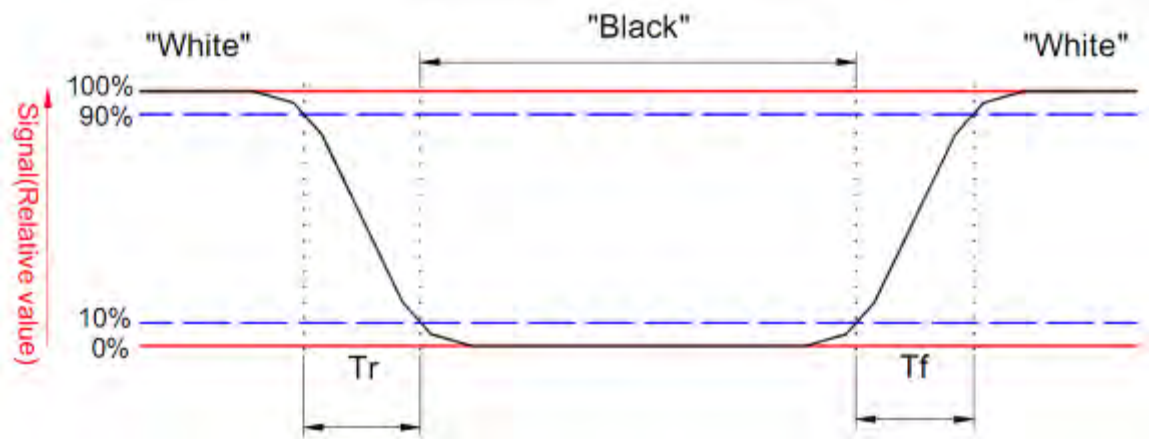
Note 2: Definition of viewing angle



Note 3: Contrast ratio is measured by Minolta CA210

Note 4: Definition of Response time

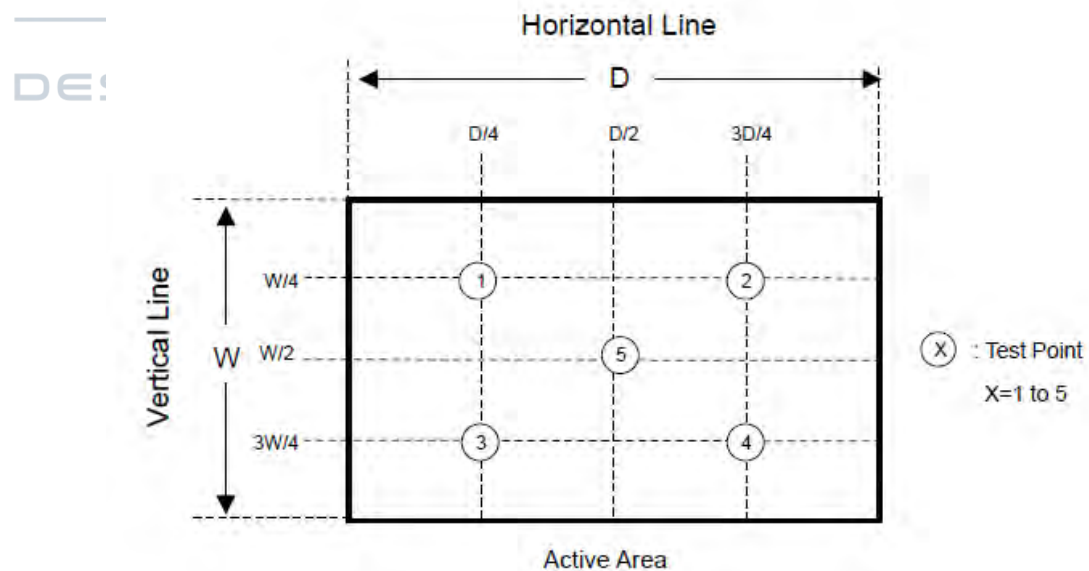
The output signals of photo detector are measured when the input signals are changed from "Full Black" to "Full White" (rising time), and from "Full White" to "Full Black" (falling time), respectively. The response time is interval between the 10% and 90% of amplitudes. Please refer to the figure as below.



Note 5: Color chromaticity and coordinates (CIE) is measured by Minolta CA210

Note 6: Center luminance is measured by Minolta CA210

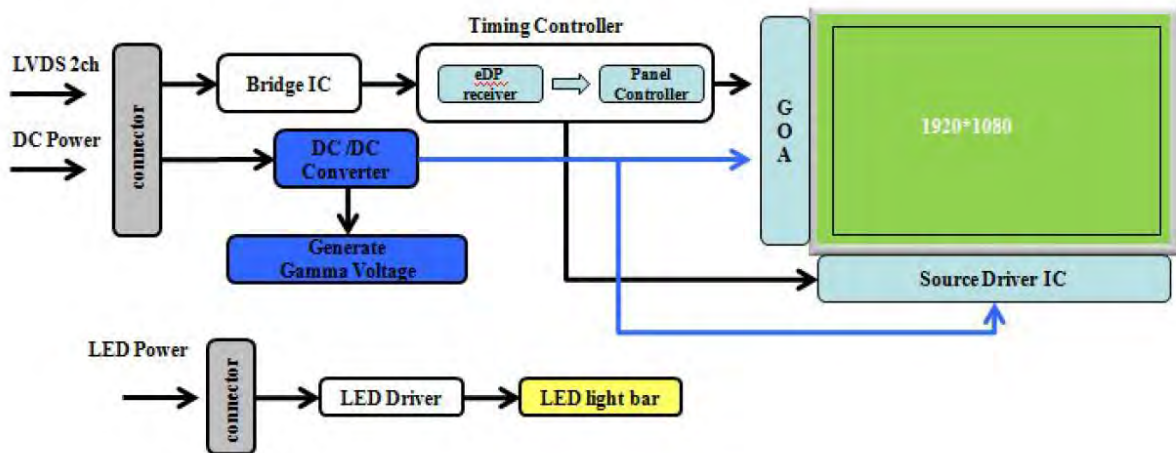
Note 7: Luminance uniformity of these 5 points is defined as below and measured by Minolta CA210



$$\text{Uniformity} = (\text{Min. Luminance of 5 points}) / (\text{Max. Luminance of 5 points})$$

3. Functional Block Diagram

The following diagram shows the functional block of the 15.6 inch Color TFT-LCD Module:



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4. Absolute Maximum Ratings

Absolute maximum ratings of the module are as following:

4.1 TFT LCD Module

Items	Symbol	Min	Max	Unit	Conditions
Power supply voltage	VDD	-0.3	4.0	Volt	
Logic input voltage	Vin	-0.3	4.0	Volt	

4.2 Backlight unit

Items	Symbol	Min	Max	Unit	Conditions
LED Current	I LED	--	600	mA	Note 1, 2

4.3 Absolute Ratings of Environment

Items	Symbol	Values			Unit	Conditions
		Min.	Typ.	Max.		
Operation temperature	T _S	-30	-	85	°C	Note 3
Operation Humidity	H _{OP}	5		90	%	
Storage temperature	T _{ST}	-40		90	°C	
Storage Humidity	H _{ST}	5		90	%	

Note 1: With in Ta= 25°C

Note 2: Permanent damage to the device may occur if exceed maximum values

- Note 3: For quality performance, please refer to IIS (Incoming Inspection Standard).

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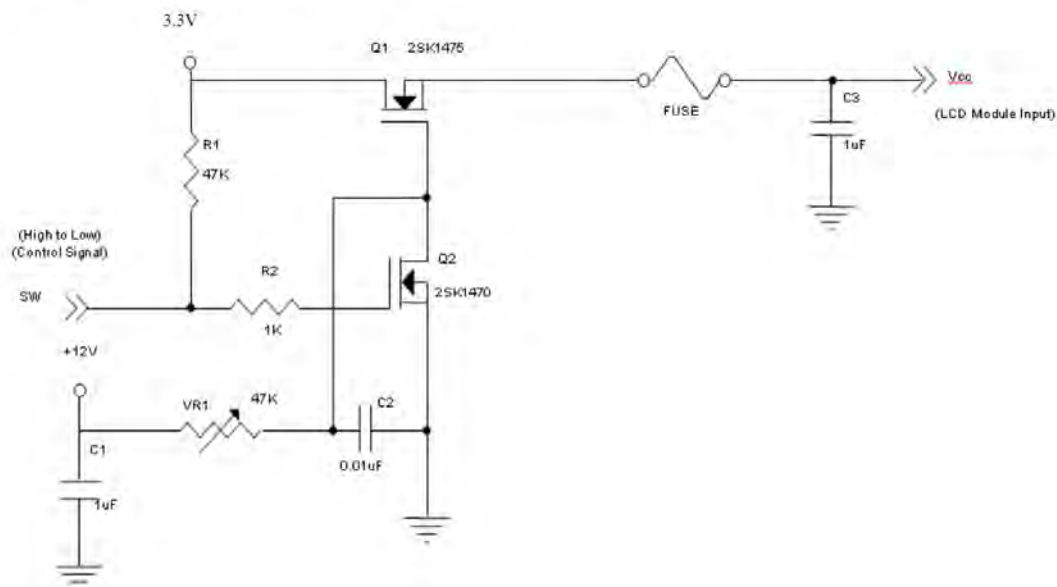
5. Electrical characteristics

5.1 TFT LCD Module Power Specification

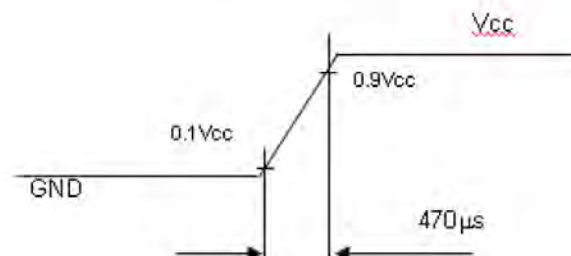
Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Supply Voltage	V_{CC}	3	3.3	3.6	V	-
Ripple Voltage	V_{RP}	-	-	150	mV	-
Rush Current	I_{RUSH}	-	-	3	A	(2)
Power Supply Current	White	-	1.22	1.5	A	(3)a
	Black	-	0.51	0.7	A	(3)b
	Vertical Stripe	-	0.82	1	A	(3)c
Power Consumption	PLCD	-	4	5	Watt	(4)
LVDS differential input voltage	V_{id}	200		600	mV	(5)
LVDS common input voltage	V_{ic}	1.0	1.2	1.4	V	(5)
LVDS terminating resistor	R_T		100		ohm	

Note (1) The ambient temperature is $T_a = 25 \pm 2^\circ\text{C}$.

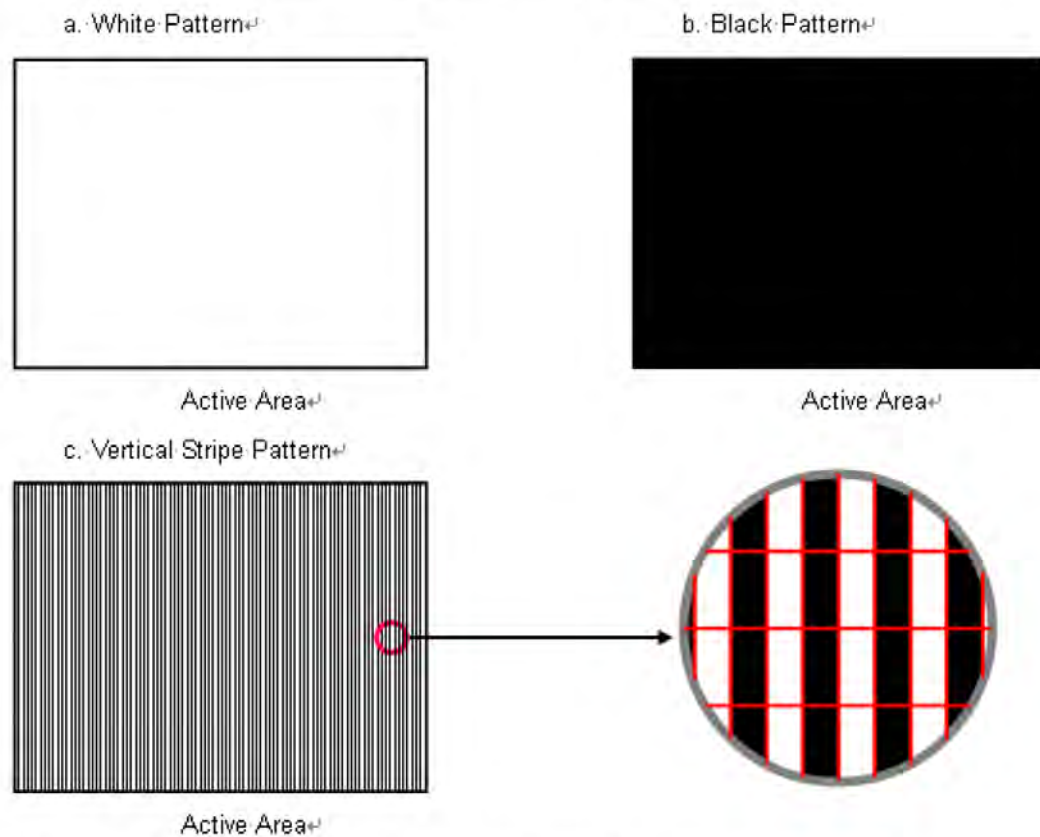
Note (2) Measurement Conditions:



VCC rising time is 470μs

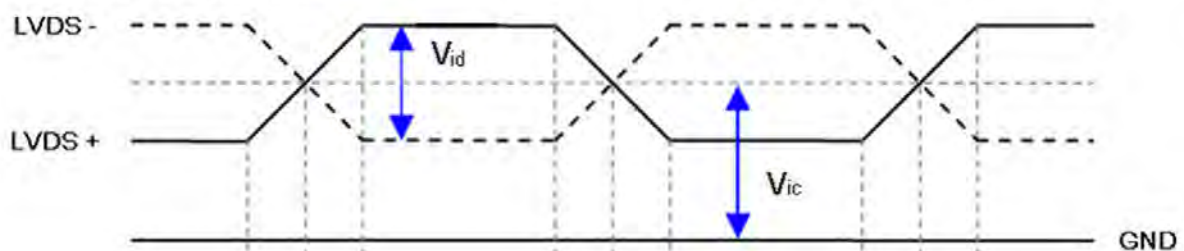


Note (3) The specified power supply current is under the conditions at $V_{CC} = 3.3\text{ V}$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, $F_r = 60\text{ Hz}$ whereas a power dissipation check pattern below is displayed.



Note (4) The power consumption is specified at the pattern with the maximum current.

Note (5) VID waveform condition



5.2 Backlight Unit

Parameter guideline is under stable conditions at 25°C (Room Temperature):

Parameter	Min	Typ	Max	Unit	Note
LED voltage (VL)		39		[V]	2
LED current (IL-channel)		300		[mA]	2,
LED Power (PL)		23.4		[W]	
LED Life Time(LTLED)		100,000		[Hour]	1

Note 1: The “LED lift time” is defined as the module brightness decrease to 50% original brightness that the ambient temperature is 25°C and typical LED Current at 300 mA/lamp.

Note 2: $PL = VL \times IL \times 2$

LED bar connector: BHSR-02VS-1 manufactured by JST

Pin no	Symbol	I/O	Description	Remark
1	VLED+	P	Backlight LED anode	Red
2	VLED-	P	Backlight LED cathode	Black

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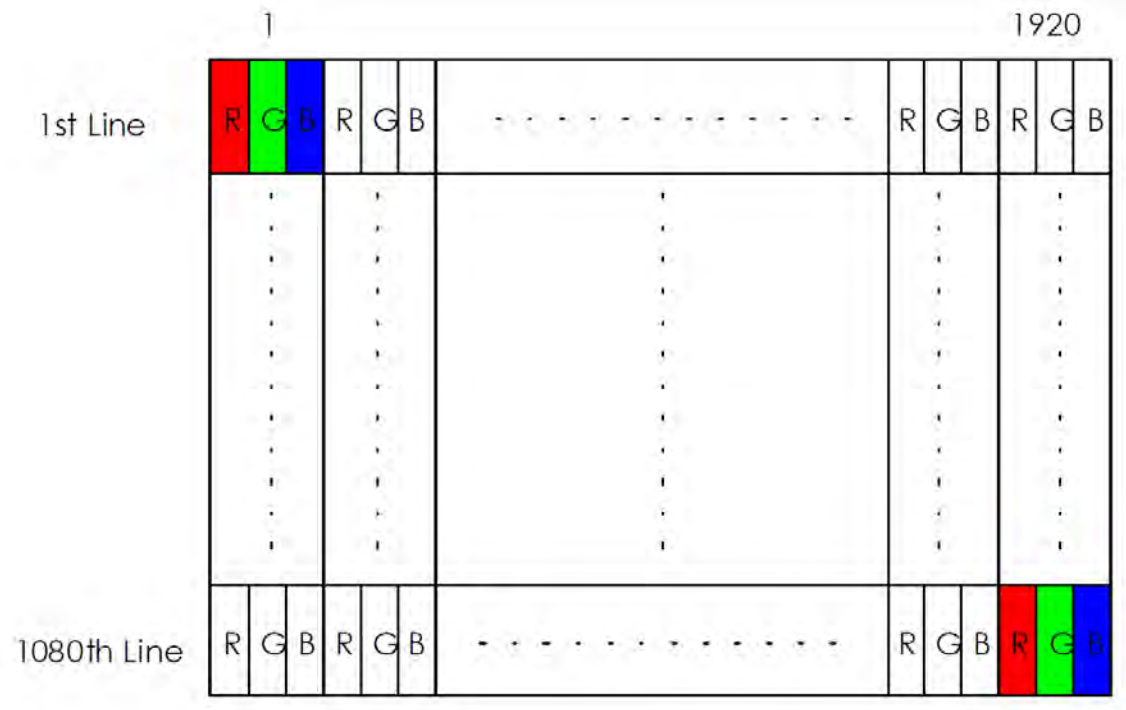
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6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



Scanning Direction

The following figures show the image seen from the front view. The arrow indicates the direction of scan.

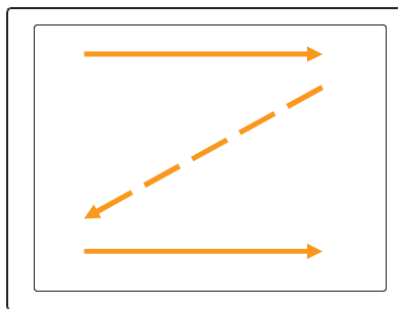


Fig. 1 Normal scan (Pin4, DPS = Low or NC)

6.2 Integration Interface Requirement

6.2.1 Connector Description

Pin	Name	Description
1	NC	Not connection, this pin should be open
2	NC	Not connection, this pin should be open
3	NC	Not connection, this pin should be open
4	NC	Not connection, this pin should be open
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	NC	Not connection, this pin should be open
10	NC	Not connection, this pin should be open
11	LCD_VCC	LCD logic and driver power 3.3V
12	LCD_VCC	LCD logic and driver power 3.3V
13	LCD_VCC	LCD logic and driver power 3.3V
14	NC	Not connection, this pin should be open
15	NC	Not connection, this pin should be open
16	NC	Not connection, this pin should be open
17	LCD GND	LCD logic and driver ground
18	RXO0-	Negative LVDS differential data input. Channel O0 (odd)
19	RXO0+	Positive LVDS differential data input. Channel O0 (odd)
20	RXO1-	Negative LVDS differential data input. Channel O1 (odd)
21	RXO1+	Positive LVDS differential data input. Channel O1 (odd)
22	RXO2-	Negative LVDS differential data input. Channel O2 (odd)
23	RXO2+	Positive LVDS differential data input. Channel O2 (odd)
24	LCD GND	LCD logic and driver ground
25	RXOC-	Negative LVDS differential clock input. (odd)
26	RXOC+	Positive LVDS differential clock input. (odd)
27	LCD GND	LCD logic and driver ground
28	RXO3-	Negative LVDS differential data input. Channel O3(odd)
29	RXO3+	Positive LVDS differential data input. Channel O3 (odd)
30	RXE0-	Negative LVDS differential data input. Channel E0 (even)
31	RXE0+	Positive LVDS differential data input. Channel E0 (even)
32	RXE1-	Negative LVDS differential data input. Channel E1 (even)
33	RXE1+	Positive LVDS differential data input. Channel E1 (even)
34	LCD GND	LCD logic and driver ground
35	RXE2-	Negative LVDS differential data input. Channel E2 (even)
36	RXE2+	Positive LVDS differential data input. Channel E2 (even)
37	RXEC-	Negative LVDS differential clock input. (even)
38	RXEC+	Positive LVDS differential clock input. (even)
39	RXE3-	Negative LVDS differential data input. Channel E3 (even)
40	RXE3+	Positive LVDS differential data input. Channel E3 (even)

Note (1) Connector Part No.: I-PEX 20455-040E-76 or equivalent.

Note (2) User's connector Part No.: I-PEX 20453-040T-03 or equivalent.

6.2.2 LVDS DATA MAPPING TABLE

LVDS Channel O0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	OG0	OR5	OR4	OR3	OR2	OR1	OR0
LVDS Channel O1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	OB1	OB0	OG5	OG4	OG3	OG2	OG1
LVDS Channel O2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	OB5	OB4	OB3	OB2
LVDS Channel O3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	OB7	OB6	OG7	OG6	OR7	OR6
LVDS Channel E0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	EG0	ER5	ER4	ER3	ER2	ER1	ER0
LVDS Channel E1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	EB1	EB0	EG5	EG4	EG3	EG2	EG1
LVDS Channel E2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	EB5	EB4	EB3	EB2
LVDS Channel E3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	EB7	EB6	EG7	EG6	ER7	ER6

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6.3 Display Timing Specification

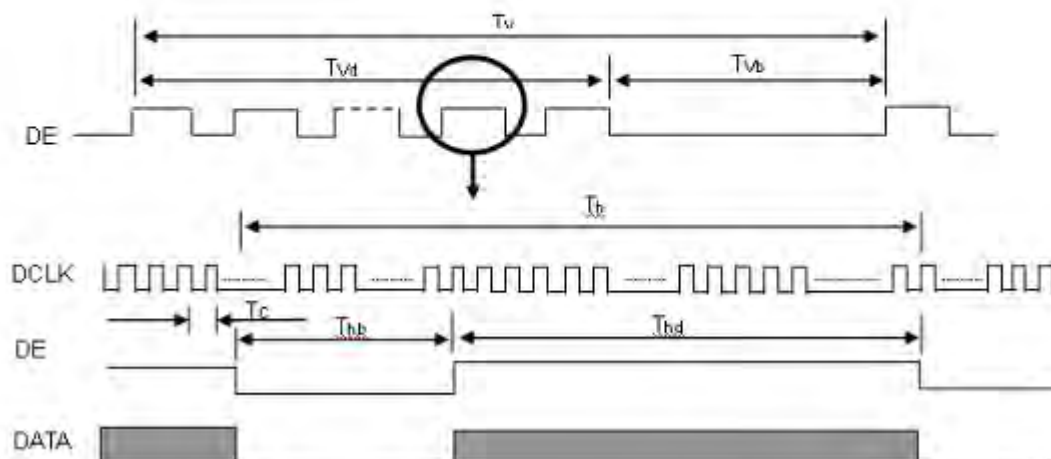
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Clock	Frequency	F_c	60	70.93	75	MHz	-
	Period	T_c		14.1		ns	
	Input cycle to cycle jitter	T_{rd}	$-0.02 \cdot T_c$		$0.02 \cdot T_c$	ns	(3)
	Input clock to data skew	TLVCCS	$-0.02 \cdot T_c$		$0.02 \cdot T_c$	ns	(4)
	Spread spectrum modulation range	F_{clk_mod}	$FC \cdot 98\%$		$FC \cdot 102\%$	MHz	(5)
	Spread spectrum modulation frequency	F_{SSM}			200	KHz	
Vertical Display Term	Frame Rate	F_r	50	60	60	Hz	$T_v = T_{vd} + T_{vb}$
	Total	T_v	1090	1110	1130	Th	-
	Active Display	T_{vd}	1080	1080	1080	Th	-
	Blank	T_{vb}	$T_v - T_{vd}$	30	$T_v - T_{vd}$	Th	-
Horizontal Display Term	Total	T_h	1050	1065	1075	Tc	$T_h = T_{hd} + T_{hb}$
	Active Display	T_{hd}	960	960	960	Tc	-
	Blank	T_{hb}	$T_h - T_{hd}$	105	$T_h - T_{hd}$	Tc	-

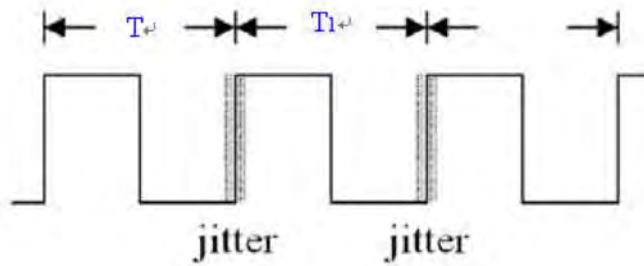
Note (1) Because this module is operated by DE only mode, Hsync and Vsync input signals are ignored.

Note (2) The $T_v(T_{vd} + T_{vb})$ must be integer, otherwise, this module would operate abnormally.

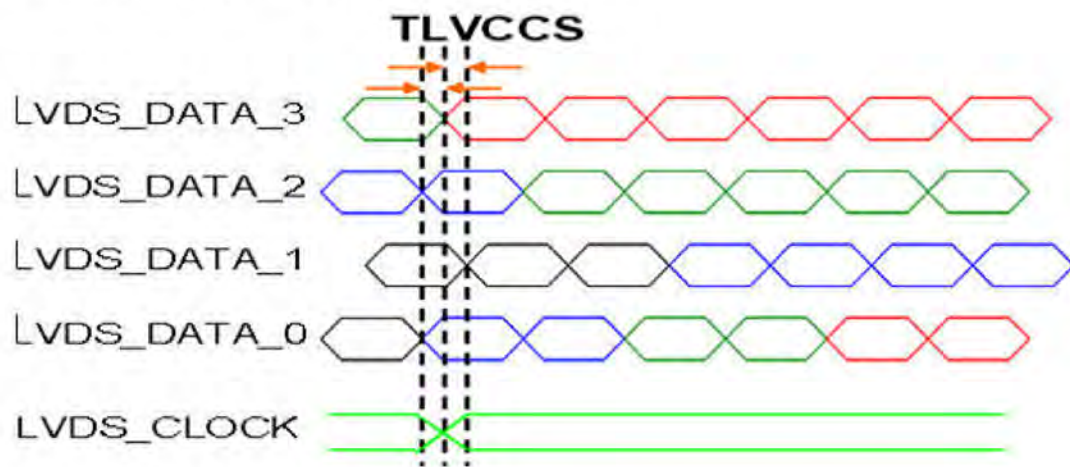
INPUT SIGNAL TIMING DIAGRAM



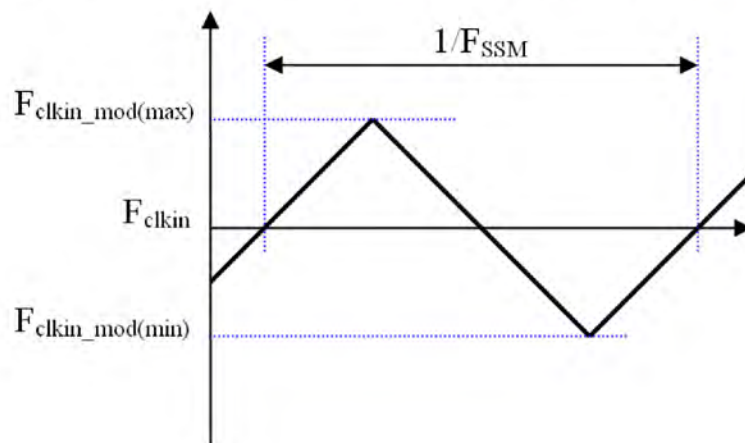
Note (3) The input clock cycle-to-cycle jitter is defined as below figures. $Trcl = |T_1 - T_0|$



Note (4) Input Clock to data skew is defined as below figures.

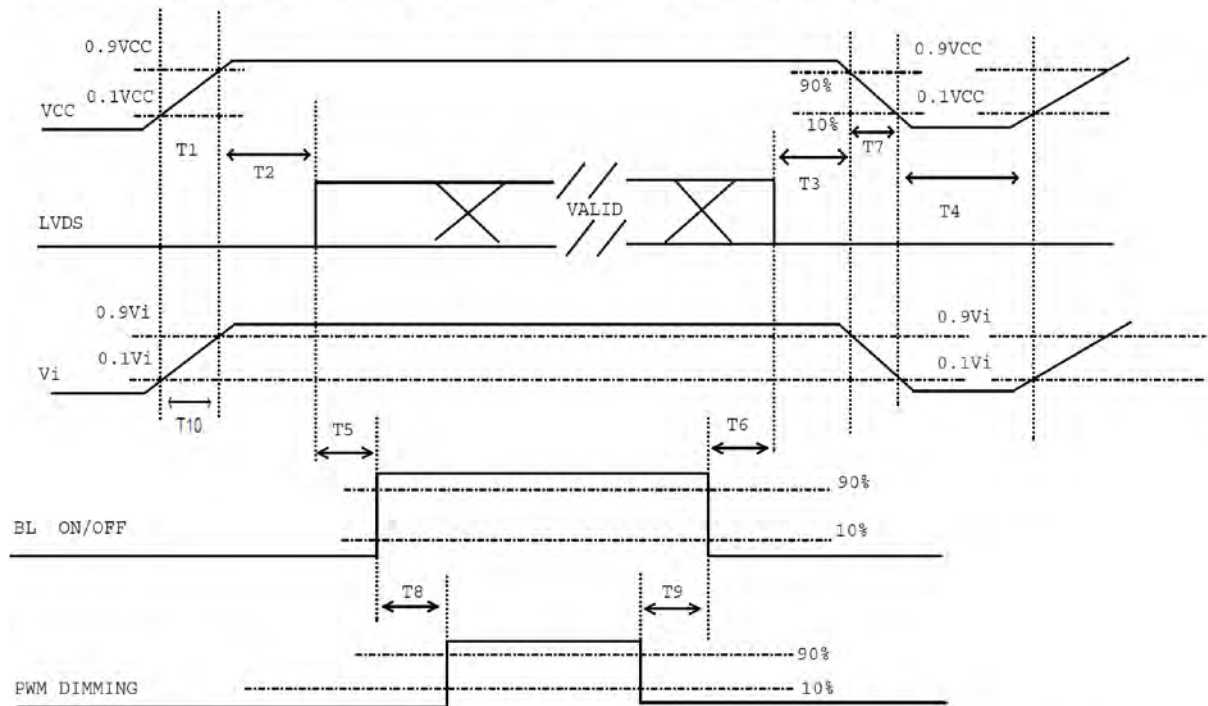


Note (5) The SSCG (Spread spectrum clock generator) is defined as below figures.



6.4 Power ON/OFF Sequence

The power sequence specifications are shown as the following table and diagram.



Timing Specifications:

Parameter	Value			Units
	Min	Typ	Max	
T1	0.5	-	10	ms
T2	0	-	50	ms
T3	0	-	50	ms
T4	500	-	-	ms
T5	450	-	-	ms
T6	20	-	-	ms
T7	10	-	300	ms
T8	10	-	-	ms
T9	10	-	-	ms
T10	20	-	-	ms

Note (1) Please avoid floating state of interface signal at invalid period.

Note (2) When the interface signal is invalid, be sure to pull down the power supply of LCD VCC to 0 V.

Note (3) The Backlight converter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight converter power must be turned off before the power supply for the logic and the interface signal is invalid.

7. Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50°C, 90%RH, 120hours	
High Temperature Operation (HTO)	Ta= 85°C, 120hours	3
Low Temperature Operation (LTO)	Ta= -30°C, 120hours	
High Temperature Storage (HTS)	Ta= 90°C, 120hours	
Low Temperature Storage (LTS)	Ta= -40°C, 120hours	
Thermal Shock Test (TST)	-20°C/30min, 60°C/30min, 100 cycles	
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (Electro Static Discharge)	Contact Discharge: $\pm 8KV$, 150pF(330 Ω) 1sec, 9 points, 25 times/ point.	
	Air Discharge: $\pm 15KV$, 150pF(330 Ω) 1sec 9 points, 25 times/ point.	

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20°C to 60°C, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: According to EN61000-4-2, ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.

Note 3: The test items are tested by open frame type chassis.

9. Mechanical Characteristic (mm)

