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MDT238001	1920x1080	LVDS Interface	TFT Module
Specification			
Version: 1		Date: 08/12/2018	
Revision			
1	06/12/2018	First issue	

Display Features	
Display Size	23.8”
Resolution	1920x1080
Orientation	Landscape
Appearance	RGB
Logic Voltage	5V
Interface	LVDS
Brightness	1000 cd/m^2
Touchscreen	---
Module Size	543.00 x 317.40 x 11.20 mm
Operating Temperature	-10°C ~ +50°C
Pinout	30 way connector
Pitch	1.00 mm

RoHS compliant

Created By	Checked By
CL	TSB
Box Quantity	Weight / Display
---	---

Display Accessories	
Part Number	**Description**
MDIB-CC1	Interconnect board for standard pitch pinouts to fine pitch wires. Providing pinouts for 2.54 pinout. 1.27, 1, 0.845, 0.8, 0.7, 0.65, 0.62, 0.6, 0.5 & 0.3 pads.

Optional Variants	
Appearances	**Voltage**

1. HANDLING PRECAUTIONS

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open or modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
10) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

2. General Description

2.1, Overview

This specification applies to the 23.8 inch color TFT-LCD module with 2-ch LVDS interface. This module supports the WUXGA -1920(H) x 1080(V) screen format and 16.7M colors (RGB 8-bits data), dual channel LVDS interface..

(Option for built-in LED driver with 24 Vdc input)

2.2 Features

- Sunlight readable display, 1000 nits.
- LED backlight
- WUXGA (1920x1080 pixels) full HD resolution
- VA mode extra wide view angle
- RoHS Compliance

2.3 Application

Industrial Application; especial for outdoor kiosk and digital signage display.

2.4 Display Specifications

Items	Unit	Specification
Screen Diagonal	inch	23.8
Active Area	mm	527.04(H) x 296.46(V)
Pixels H x V	pixels	1920(x3) x 1080
Pixels Pitch	um	274.5(per one triad) x 274.5
Pixel Arrangement		RGB Vertical stripe
Display mode		VA mode, normally black
White luminance (center)	Cd/m^2	1000 (Typ.)
Contrast ratio		3,000 (Typ.)
Optical Response Time	msec	12 ms (Typ. on/off)
Normal Input Voltage VDD	Volt	5
Power Consumption (VDD Line + LED lines)	Watt	33.8W (Typ.) VDD line:5.0 W, all white pattern; LED=28.8 W
Weight	Grams	2280 (Typ.)
Physical size	mm	543.0 x 317.4 x11.2 (Typ.)
Electrical Interface		Dual Channel LVDS
Support Colors		16.7 M colors (RGB 8-bits)
Surface Treatment		Anti-Glare, 3H
Temperature range Operating Storage (Shipping)	 ^0C ^0C	 -10 ~ 50 (70C TFT surface temperature) -20 ~ 60
RoHS Compliance		RoHS Compliance

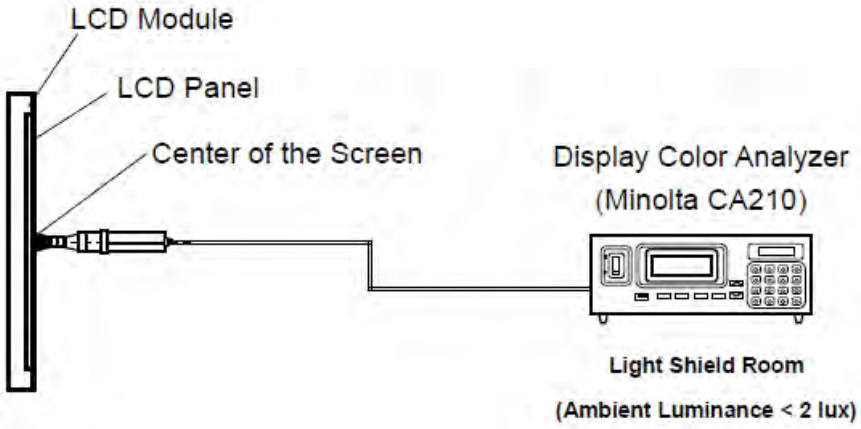
2.5 Optical Characteristics

The following optical characteristics are measured under stable condition at 25 ^{0}C

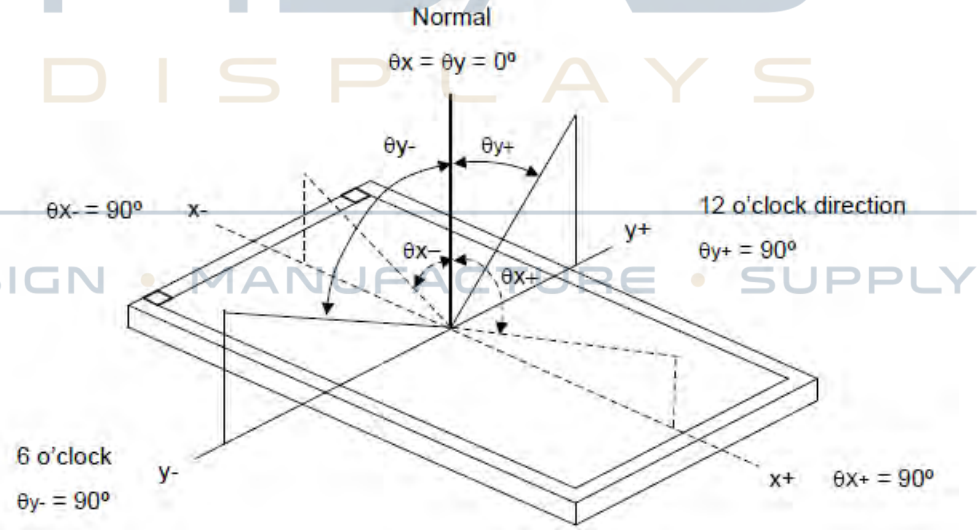
Items	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing angle	Deg.	Horizontal (Right) CR=10 (Left)	150	178		2
		Vertical (Up) CR=10 (Down)	150	178		
Contrast Ratio		Normal Direction	1500	3000		3
Response Time	msec	G to G		20		4
Color / Chromaticity Coordinates (CIE)		Red x	Typ -0.04	0.65	Typ +0.04	5
		Red y		0.33		
		Green x		0.32		
		Green y		0.62		
		Blue x		0.15		
		Blue y		0.08		
Color coordinates (CIE) White		White x		0.31		
		White y		0.34		
Center Luminance	Cd/m^2		800	1000		6
Luminance Uniformity	%		60	70		7
Crosstalk (in 60 Hz)	%				1.5	
Flicker	dB				-20	

Note 1: Measurement method

The LCD module should be stabilized at given temperature for 0.5 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.



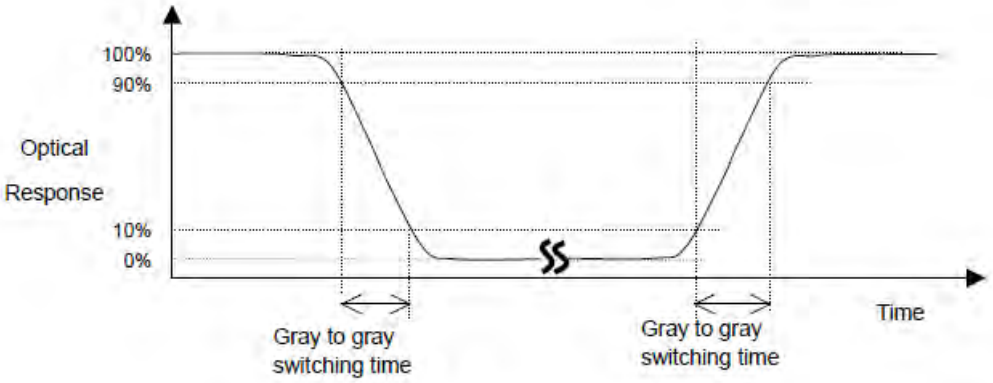
Note 2: Definition of viewing angle



Note 3: Contrast ratio is measured by Minolta CA210

Note 4: Definition of Response time

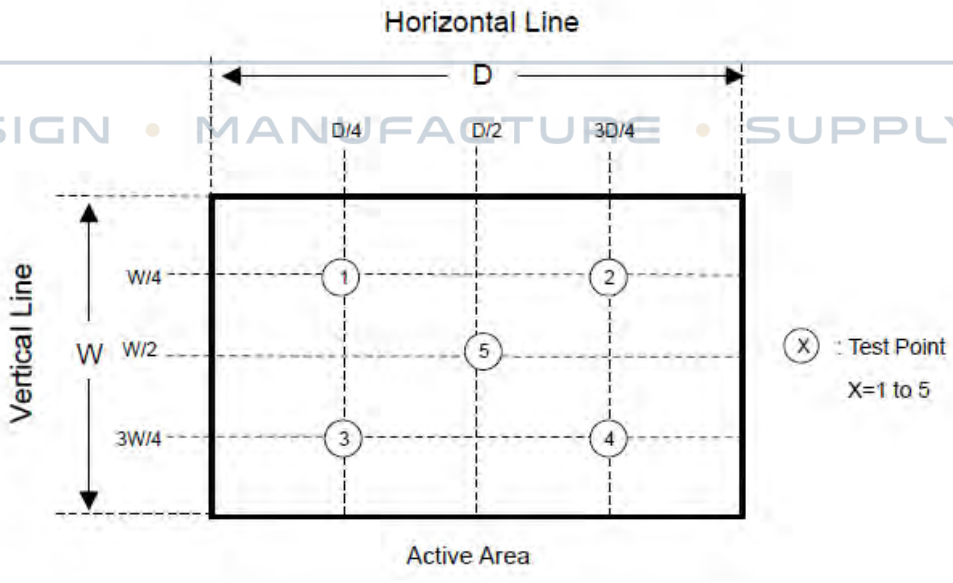
The output signals of photo detector are measured when the input signals are changed from “Full Black” to “Full White” (rising time), and from “Full White” to “Full Black” (falling time), respectively. The response time is interval between the 10% and 90% of amplitudes. Please refer to the figure as below.



Note 5: Color chromaticity and coordinates (CIE) is measured by Minolta CA210

Note 6: Center luminance is measured by Minolta CA210

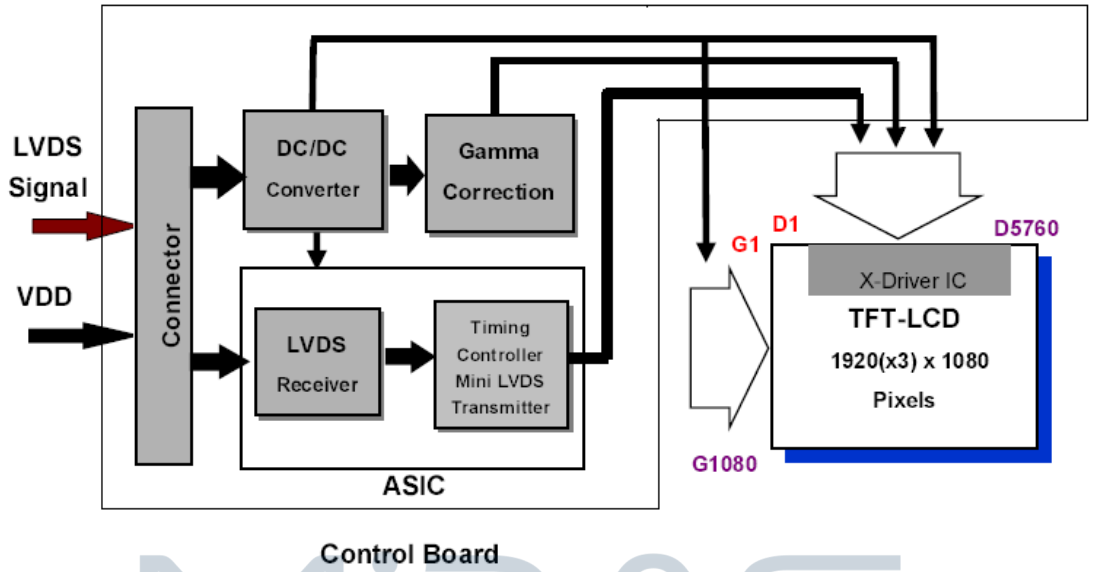
Note 7: Luminance uniformity of these 5 points is defined as below and measured by Minolta CA210



Uniformity = (Min. Luminance of 5 points) / (Max. Luminance of 5 points)

3. **Functional Block Diagram**

The following diagram shows the functional block of the 23.8 inches Color TFT-LCD Module:



I/F PCB Interface:

P-TWO 187043-3009

STM MSBKT2407P30HB

Mating Type:

JAE FI-X30HL (Locked Type)

4. Absolute Maximum Ratings

Absolute maximum ratings of the module are as following:

4.1 TFT LCD Module

Items	Symbol	Min	Max	Unit	Conditions
Logic/ LCD drive voltage	VDD	0	6.0	Volt	Note 1, 2

4.2 Backlight unit

Items	Symbol	Min	Max	Unit	Conditions
LED Current	I LED		120	mA	Note 1, 2

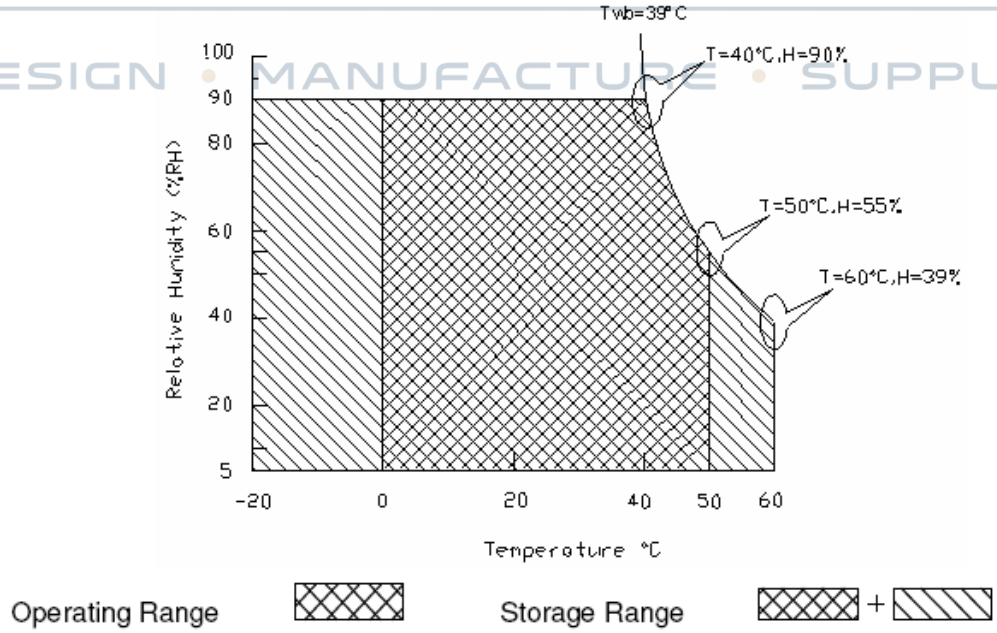
4.3 Absolute Ratings of Environment

Items	Symbol	Values			Unit	Conditions
		Min.	Typ.	Max.		
Operation temperature	T_{OP}	-10	-	50	^{0}C	Note 3
Operation Humidity	H_{OP}	5		90	%	
Storage temperature	T_{ST}	-20		60	^{0}C	
Storage Humidity	H_{ST}	5		90	%	

Note 1: With in Ta= 25℃

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to IIS (Incoming Inspection Standard).



5. Electrical characteristics

5.1 TFT LCD Module

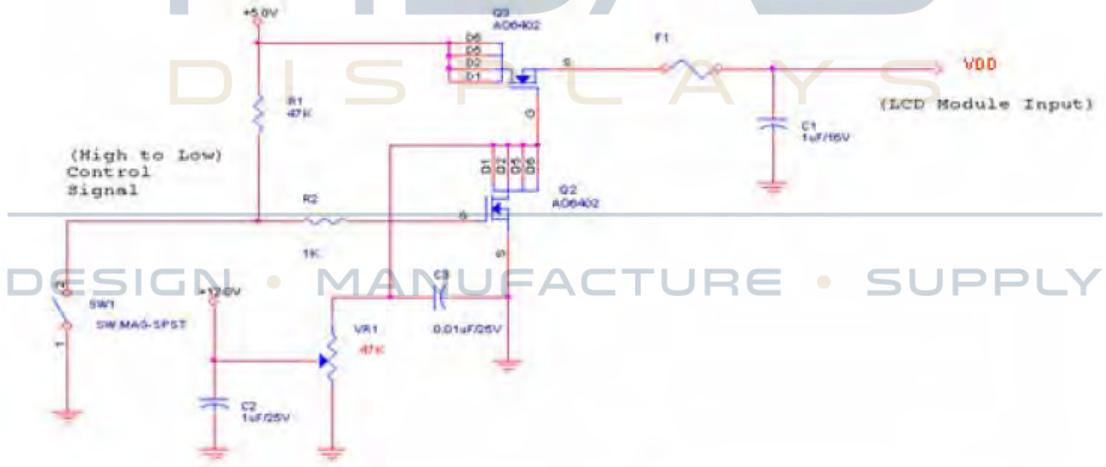
5.1.1 Power Specification

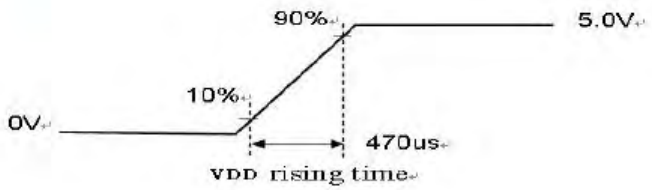
Input power specifications are as follows

Symbol	Parameter	Min	Typ.	Max	Unit	Conditions
VDD	Logic/ LCD Drive Voltage	4.5	5	5.5	Volt	+/- 10%
IDD	Input current		1.0	1.2	A	VDD=5V, All black pattern. At 60Hz, +30%
PDD	VDD power		5.0	6.0	W	VDD=5V, All black pattern. At 60Hz,
IRush	Inrush current			3	A	Note 1
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			500	mV p-p	VDD=5V, All black pattern. At 75Hz,

Note 1: Measurement conditions:

The duration of rising time of input power is 470 us.





5.1.2 Signal Electrical Characteristics

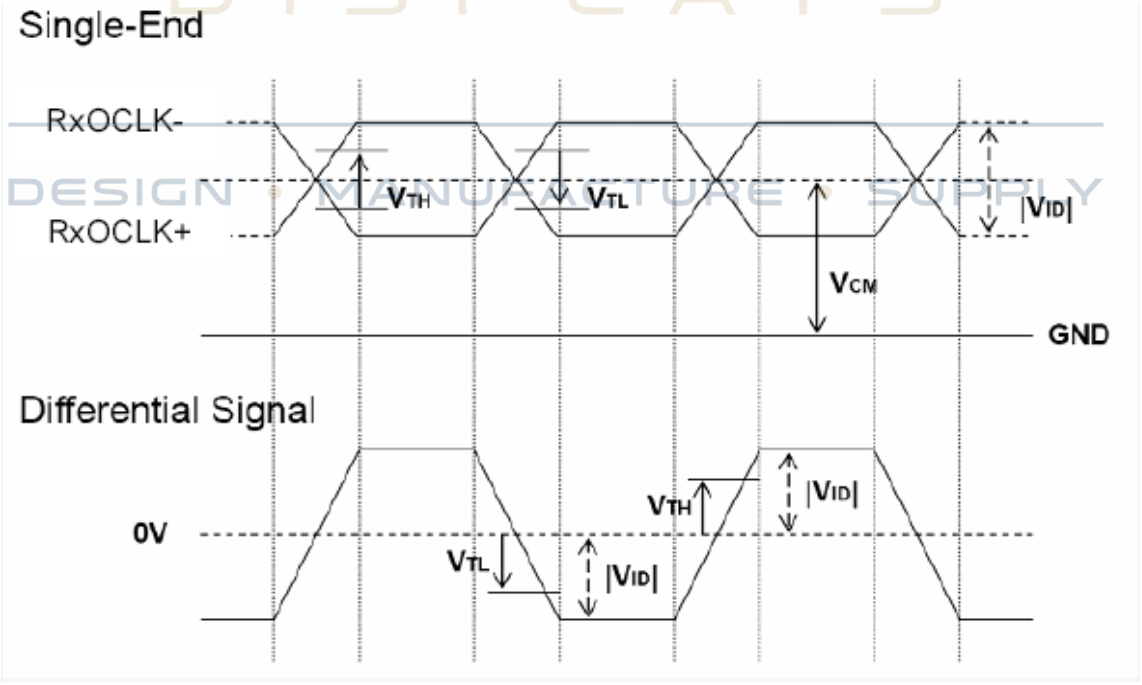
Input signal shall be low or Hi-Z state when VDD is off. Please refer to specification of SN75LVDS82DGG (Texas Instruments) in detail.

1. DC Characteristics of each signal are as following:

Characteristics of each signal are as following:

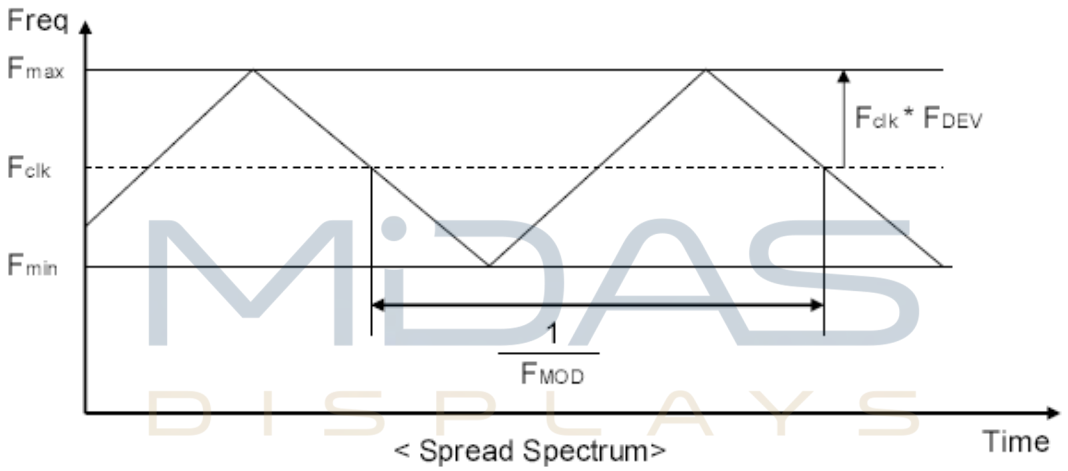
Symbol	Parameter	Min	Typ	Max	Unit	Condition
VTH	Differential Input High Threshold		+50	+100	mV	VICM = 1.2V NOTE 1
VTL	Differential Input Low Threshold	-100	-50		mV	VICM = 1.2V NOTE 1
|VID|	Input Differential Voltage	100		600	mV	NOTE 1
VICM	Differential Input Common Mode Voltage	+1.0	+1.2	+1.5	V	VTH-VTL = 200mV(MAX) NOTE 1

Note 1: LVDS Signal Waveform



2. AC Characteristics

Symbol	Description	Min	Max	Unit	Remark
F_{DEV}	Maximum deviation of input clock frequency during Spread Spectrum	-	± 3	%	
F_{MOD}	Maximum modulation frequency of input clock during Spread Spectrum	-	200	KHz	



Fclk: LVDS Clock Frequency

5.2 Backlight Unit

Parameter guideline is under stable conditions at 25℃ (Room Temperature):

Parameter	Min	Typ	Max	Unit	Note
LED voltage (VL)		36		[V]	
LED current (IL)		400		[mA]	,
LED power (PL)		28.8		W	
LED Life Time(LTLED)		50000		[Hour]	1

Note 1: The “LED lift time” is defined as the module brightness decrease to 50% original brightness that the ambient temperature is 25℃ and typical LED Current at 400 mA .

Note 2: PL=VL x IL x 2

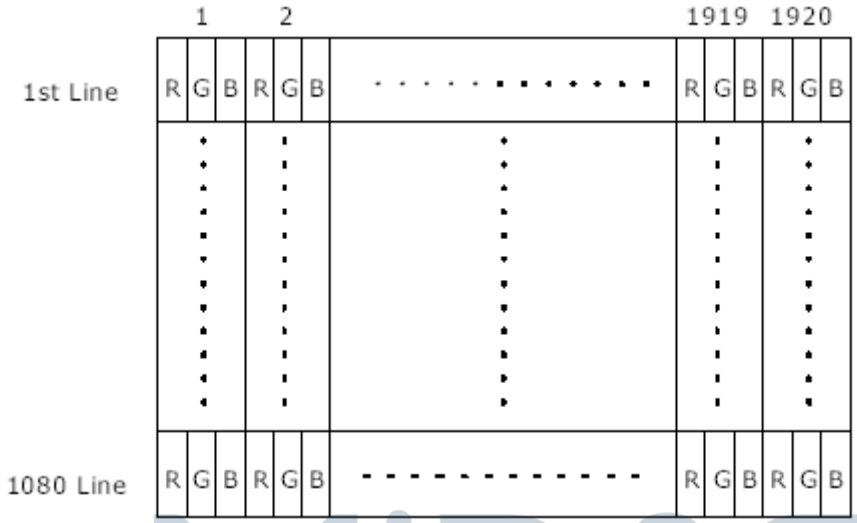
LED driver (Option)

Parameter	Min	Typ	Max	Unit	Note
Input voltage		24		[V]	
Input current			2.5	[A]	,

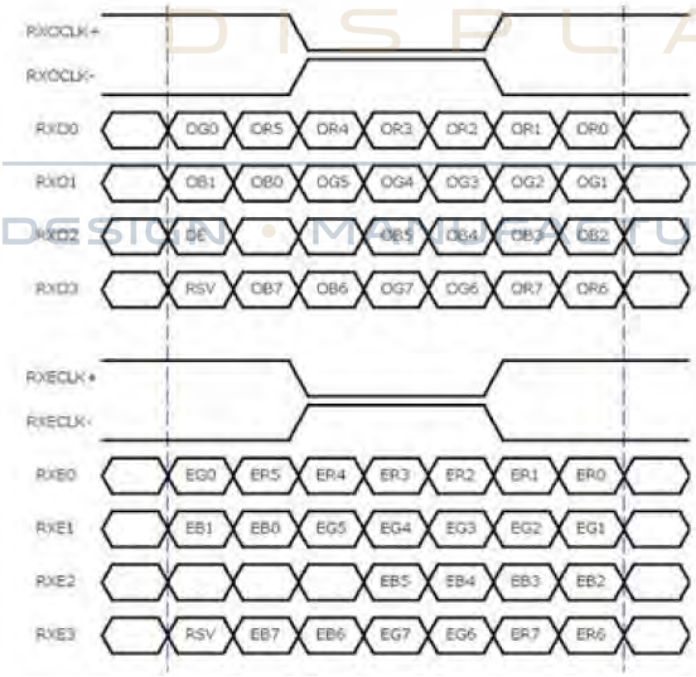
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 LVDS Data Format



8 Bit Color Bit Order			
MSB	R7	G7	B7
	R6	G6	B6
	R5	G5	B5
	R4	G4	B4
	R3	G3	B3
	R2	G2	B2
	R1	G1	B1
LSB	R0	G0	B0

Note 1: a. O = “Odd Pixel Data” E = “Even Pixel Data”

b. Refer to 3.4.1 LCD pixel format, the 1st data is 1 (Odd Pixel Data), the 2nd data is 2 (Even Pixel Data) and the

last data is 1920 (Even Pixel Data).

6.2 Color versus input data

The following table is for color versus input data (8bit).

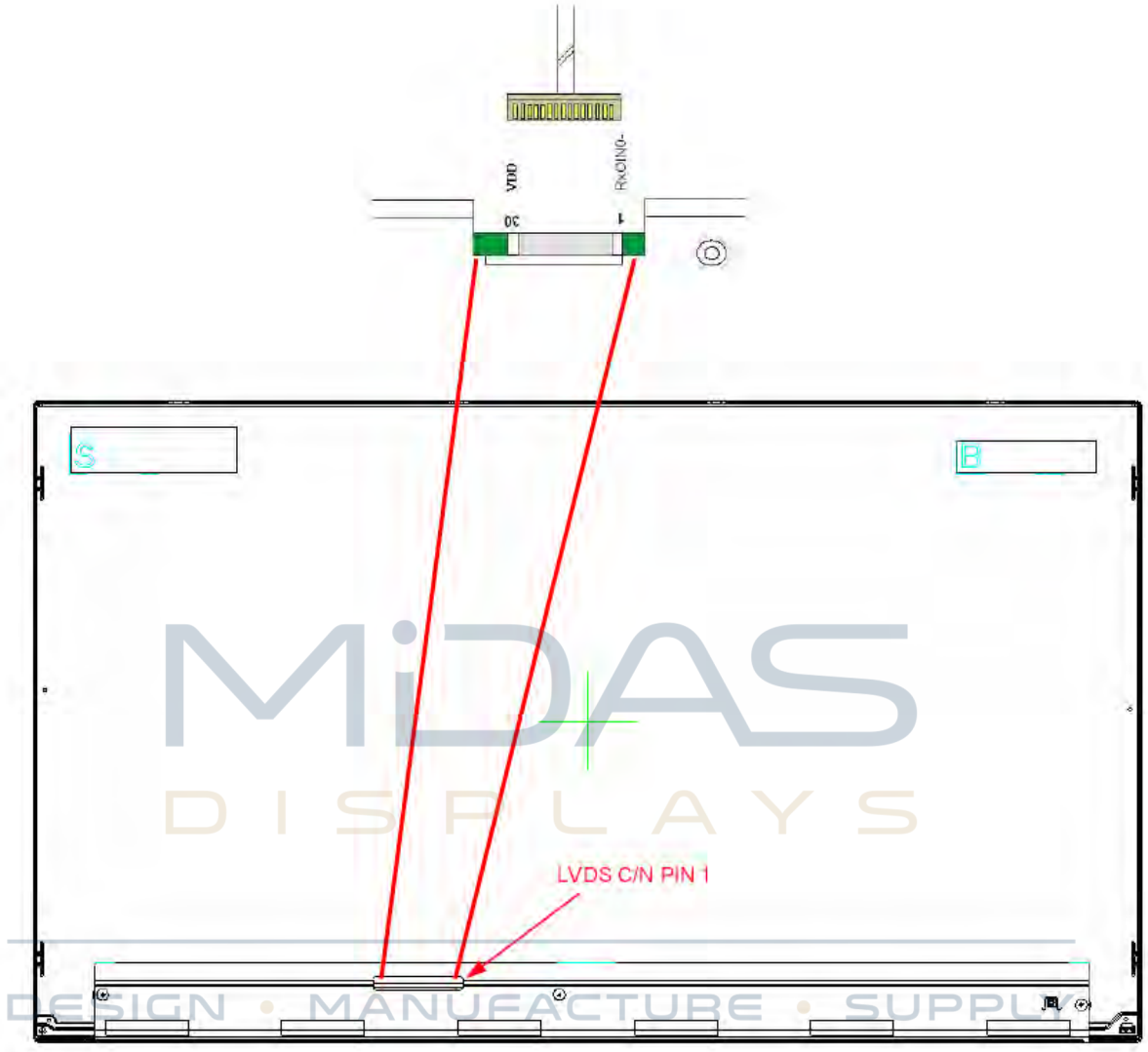
The higher the gray level, the brighter the color.

Color	Gray Level	Color Input Data																								Remark
		RED data (MSB:R7, LSB:R0)								GREEN data (MSB:G7, LSB:G0)								BLUE data (MSB:B7, LSB:B0)								
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	
Black	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
White	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray 127	-	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	
Red	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Green	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Blue	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	

6.3 Signal Description

PIN#	Signal Name	DESCRIPTION
1	RxO0-	Negative LVDS differential data input (Odd data)
2	RxO0+	Positive LVDS differential data input (Odd data)
3	RxO1-	Negative LVDS differential data input (Odd data)
4	RxO1+	Positive LVDS differential data input (Odd data)
5	RxO2-	Negative LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG)
6	RxO2+	Positive LVDS differential data input (Odd data, H-Sync,V-Sync,DSPTMG)
7	GND	Power Ground
8	RxOCLK-	Negative LVDS differential clock input (Odd clock)
9	RxOCLK+	Positive LVDS differential clock input (Odd clock)
10	RxO3-	Negative LVDS differential data input (Odd data)
11	RxO3+	Positive LVDS differential data input (Odd data)
12	RxE0-	Negative LVDS differential data input (Even data)
13	RxE0+	Positive LVDS differential data input (Even data)
14	GND	Power Ground
15	RxE1-	Negative LVDS differential data input (Even data)
16	RxE1+	Positive LVDS differential data input (Even data)
17	GND	Power Ground
18	RxE2-	Negative LVDS differential data input (Even data)
19	RxE2+	Positive LVDS differential data input (Even data)
20	RxECLK-	Negative LVDS differential clock input (Even clock)
21	RxECLK+	Positive LVDS differential clock input (Even clock)
22	RxE3-	Negative LVDS differential data input (Even data)
23	RxE3+	Positive LVDS differential data input (Even data)
24	GND	Power Ground
25	NC	Do not connect (for test only)
26	NC	Do not connect (for test only)
27	NC	Do not connect (for test only)
28	VDD	Power +5V
29	VDD	Power +5V
30	VDD	Power +5V

Note 1: Start from right side



6.4. Timing Characteristics

It only support DE mode, and the input timing are shown as the following table.

Symbol	Description		Min.	Typ.	Max.	Unit.	Remark
Tv	Vertical sction	Period	1094	1130	1836	Th	
Tdisp(v)		Active	1080	1080	1080	Th	
Tblk (v)		Blanking	14	50	756	Th	
Fv		Frequency	50	60	76	Hz	
Th	Horizontal section	Period	1000	1050	1678	Tclk	
Tdisp (h)		Active	960	960	960	Tclk	
Tblk (h)		Blanking	44	90	718	Tclk	
Fh		Frequency	53.7	67.8	90	KHz	Note 1
Tclk	LVDS clock	Period	11.2	14.0	18.6	Ns	1/ Fclk
Fclk		Frequency	53.7	71.2	90.0	MHz	Note 2

Note 1: The equation is listed as following. Please don't exceed the above recommended value.

Fh (Min.) = Fclk (Min.) / Th (Min.);

Fh (Typ.) = Fclk (Typ.) / Th (Typ.);

Fh (Max.)= Fclk (Max.) / Th (Min.);

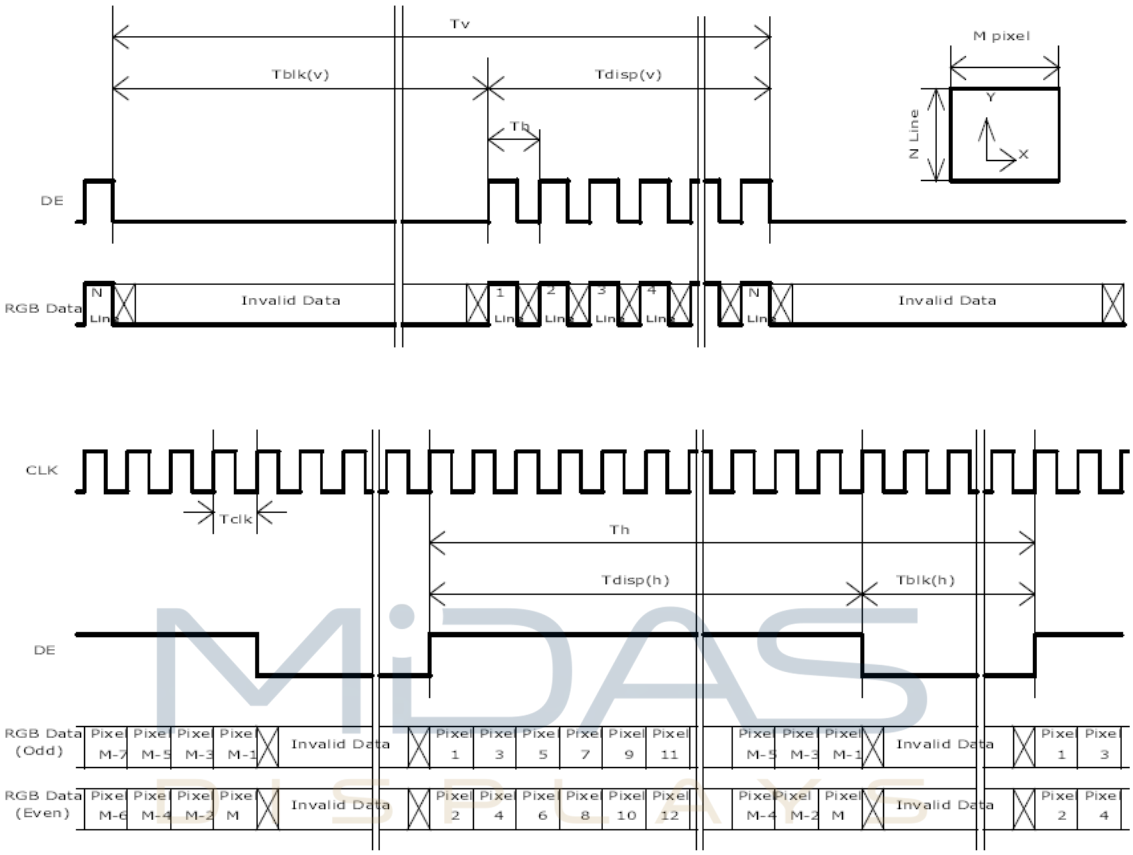
Note 2: The equation is listed as following. Please don't exceed the above recommended value.

Fclk (Min.) = Fv (Min.) x Th (Min.) x Tv (Min.);

Fclk (Typ.) = Fv (Typ.) x Th (Typ.) x Tv (Typ.);

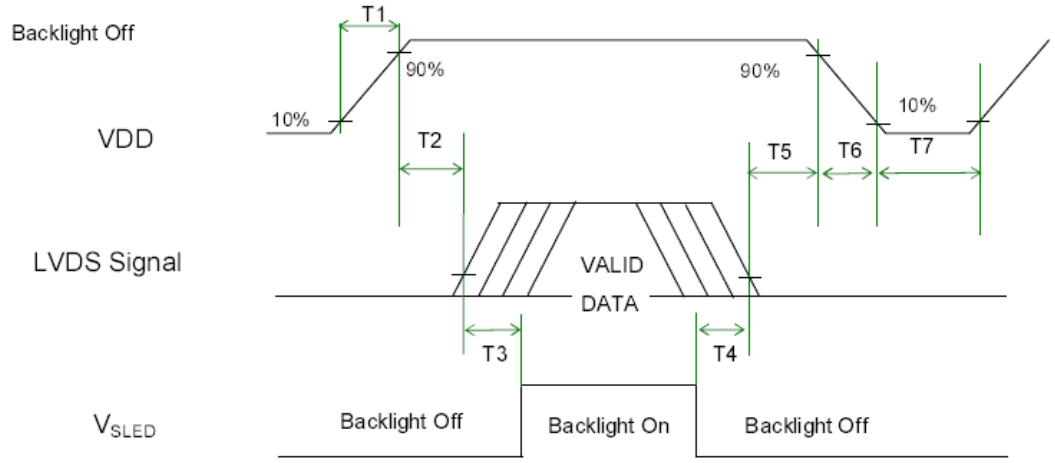
Fclk (Max.) = Fv (Max.) x Th (Typ.) x Tv (Typ.);

6.5 Timing Diagram



6.5 Power ON/OFF Sequence

VDD power, LVDS signal and backlight on/off sequence are as following. LVDS signals from any system shall be Hi-Z state when VDD is off.



Power Sequence timing

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T1	0.5	-	10	ms	
T2	0	-	50	Ms	
T3	500	-	-	Ms	
T4	100	-	-	Ms	
T5	0		50	Ms	Note1
T6	5	-	150	Ms	Note 2
T7	1000	-	-	ms	

Note1 : Recommend setting T5 = 0ms to avoid electronic noise when VDD is off.

Note2 : During T5 and T6 period , please keep the level of input LVDS signals with Hi-Z state

7.0 Connector & Pin Assignment

Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module (CN1)

Connector Name / Designation	Interface Connector / Interface card
Manufacturer	P-TWO, STM
Type Part Number	P-TWO 187034-3009 STM MSBKT2407P30HB
Mating Housing Part Number	FI-X30HL(Locked type)

7.1.1 Pin Assignment

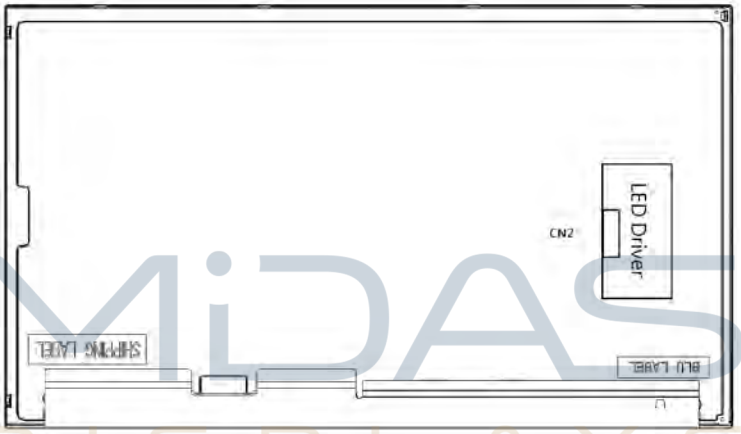
Pin#	Signal Name	Pin#	Signal Name
1	RxOIN0-	2	RxOIN0+
3	RxOIN1-	4	RxOIN1+
5	RxOIN2-	6	RxOIN2+
7	GND	8	RxOCLK-
9	RxOCLK+	10	RxOIN3-
11	RxOIN3+	12	RxEIN0-
13	RxEIN0+	14	GND
15	RxEIN1-	16	RxEIN1+
17	GND	18	RxEIN2-
19	RxEIN2+	20	RxECLK-
21	RxECLK+	22	RxEIN3-
23	RxEIN3+	24	GND
25	NC	26	NC
27	NC	28	VDD
29	VDD	30	VDD

7.2 Backlight Unit

Pin No.	Symbol	I/O	Function	Remark
1	VLED+	P	Power for LED backlight anode	White
2	VLED-	P	Power for LED backlight cathode	Black

LED Light Bar Connector is used for the integral backlight system. The recommended model is BHSR-02VS-1 manufactured by JST. (2 connectors)

(Option) CN2 Position (built-in LED driver)



(Option) CN2 Pin assignment

CN1: CviLux CI0106M1HR0-LF or Equivalent

Pin No	Symbol	**Description**
1	VIN	DC +24V
2	VIN	DC +24V
3	ON/OFF	OFF=0V
		ON=+3V (5V max)
4	DIM	Dimming Control PWM (180 ~220 Hz)
5	GND	GROUND
6		GROUND

8. Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50℃, 80%RH, 120hours	
High Temperature Operation (HTO)	Ta= 50℃, 50%RH, 120hours	3
Low Temperature Operation (LTO)	Ta= -10℃, 120hours	
High Temperature Storage (HTS)	Ta= 60℃, 120hours	
Low Temperature Storage (LTS)	Ta= -20℃, 120hours	
Drop Test	Height: 60 cm, package test	
Thermal Shock Test (TST)	-20℃/30min, 60℃/30min, 100 cycles	
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (ElectroStatic Discharge)	Contact Discharge: ± 8KV, 150pF(330Ω) 1sec, 9 points, 25 times/ point.	
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 9 points, 25 times/ point.	

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20℃ to 60℃, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.

Note 3: The test items are tested by open frame type chassis.

10. Mechanical Characteristic