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MDT270000C	3840x2160	EDP Interface	TFT Module

Specification

Version: 1	Date: 22/10/2021

Revision

1	20/10/2021	First issue

Display Features	
Display Size	27”
Resolution	3840x2160
Orientation	Landscape
Appearance	RGB
Logic Voltage	10V
Interface	EDP
Brightness	1400 cd/m^2
Touchscreen	CTP
Module Size	608.80 x 349.40 x 50.00 mm
Operating Temperature	-10°C ~ +50°C
Pinout	30 way connector
Pitch	0.50 mm

RoHS compliant

Created By	Checked By
CL	TSB
Box Quantity	Weight / Display
---	---

Display Accessories

Part Number	Description
MDIB-CC1	Interconnect board for standard pitch pinouts to fine pitch wires. Providing pinouts for 2.54 pinout. 1.27, 1, 0.845, 0.8, 0.7, 0.65, 0.62, 0.6, 0.5 & 0.3 pads.

Optional Variants

Appearances	Voltage

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open or modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
10) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

2. General Description

2.1 Overview

This specification applies to the Color Active Matrix Liquid Crystal Display composed of a TFT-LCD display a LED backlight system. The screen format is intended to support UHD (3840(H) x 2160(V) screen and 1.07B colors.
LED driving board for backlight unit is included.

2.2 Features

- High brightness display, 1500nits by LED backlight.
- Long operation lifetime BLU design
- Wide view angle
- eDP interface
- RoHS Compliance

2.3 Application

Industrial applications.

2.4 Display specifications

Items	Unit	Specification
Screen Diagonal	mm	27.0inch
Active Area	mm	596.74 (H) X 335.66(V)
Pixels H x V	pixels	3840 x3(RGB) x 2160
Pixels Pitch	um	155.4 (per one triad) x 155.4
Pixel Arrangement		RGB Vertical stripe
Display mode		Normally Black
White luminance (center)	Cd/m^2	1400 (Typ)
Contrast ratio		1300 : 1
Optical Response Time	msec	14 ms (Typ. On/off)
Normal Input Voltage VDD	Volt	10.0
Power Consumption (Vcc Line + LED backlight)	Watt	117.2W (VDD line= 9.2 W; LED lines= 108 W)
Weight	Grams	TBD
Physical size	mm	608.8 (W)×349.4 (H)×50.0 (D)
Electrical Interface		eDP
Support colors		1.07B colors
Surface Treatment		Anti-glare and hard-coating 3H
Temperature range Operating Storage	 ^0C ^0C	 -10 ~ 50 -20 ~ 60
RoHS Compliance		RoHS Compliance

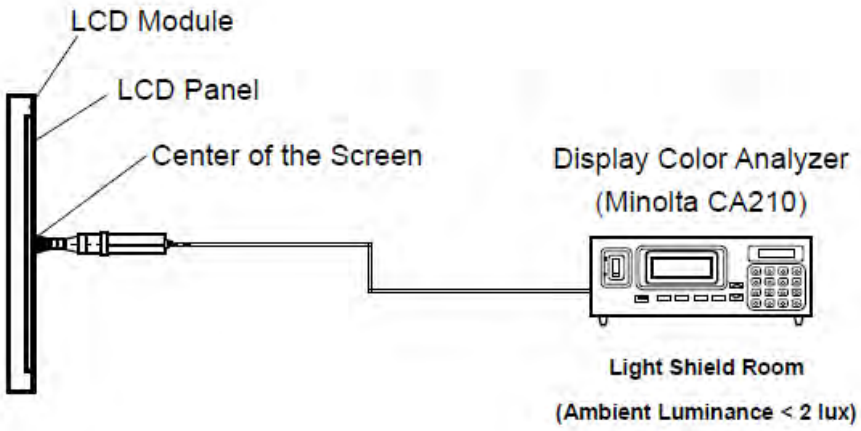
2.5 Optical characteristics

The following optical characteristics are measured under stable condition at 25 ^{0}C

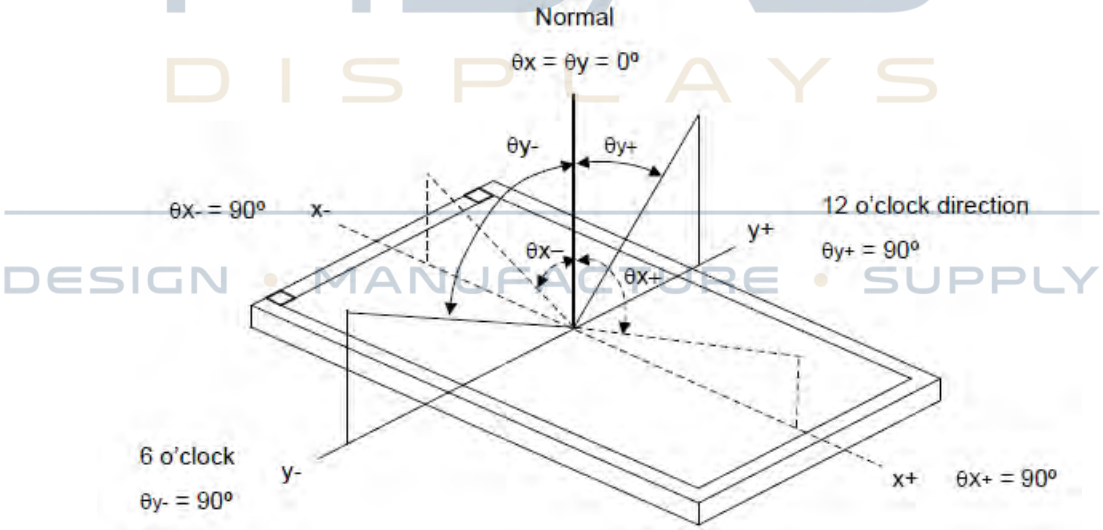
Items	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing angle	Deg.	Horizontal (Right) CR=10 (Left)	170	178		2
		Vertical (Up) CR=10 (Down)	170	178		
Contrast Ratio		Normal Direction	910	1300		3
Response Time	msec	Raising + Falling		14	25	4
Color / Chromaticity Coordinates (CIE)		Red x	-0.05	0.647	+0.05	5
		Red y		0.314		
		Green x		0.277		
		Green y		0.678		
		Blue x		0.154		
		Blue y		0.053		
Color coordinates (CIE) White		White x		0.313		
		White y		0.329		
Center Luminance	Cd/m^2		1200	1400		6
Luminance Uniformity	%		70	75		7
Color Gamut (CIE1931)	sRGB			(99)		
Color Gamut (CIE1976)	DCI-P3			(95)		
Crosstalk (in 60 Hz)	%				1.5	
Flicker	dB				-20	

Note 1: Measurement method

The LCD module should be stabilized at given temperature for 0.5 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.



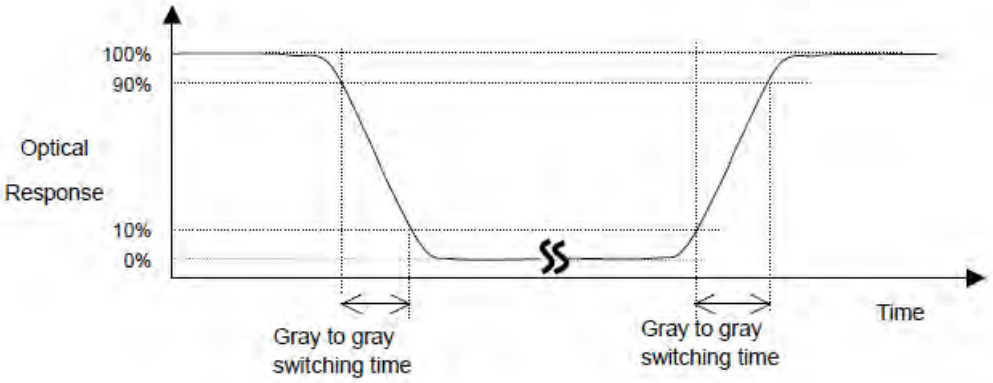
Note 2: Definition of viewing angle



Note 3: Contrast ratio is measured by Minolta CA210

Note 4: Definition of Response time

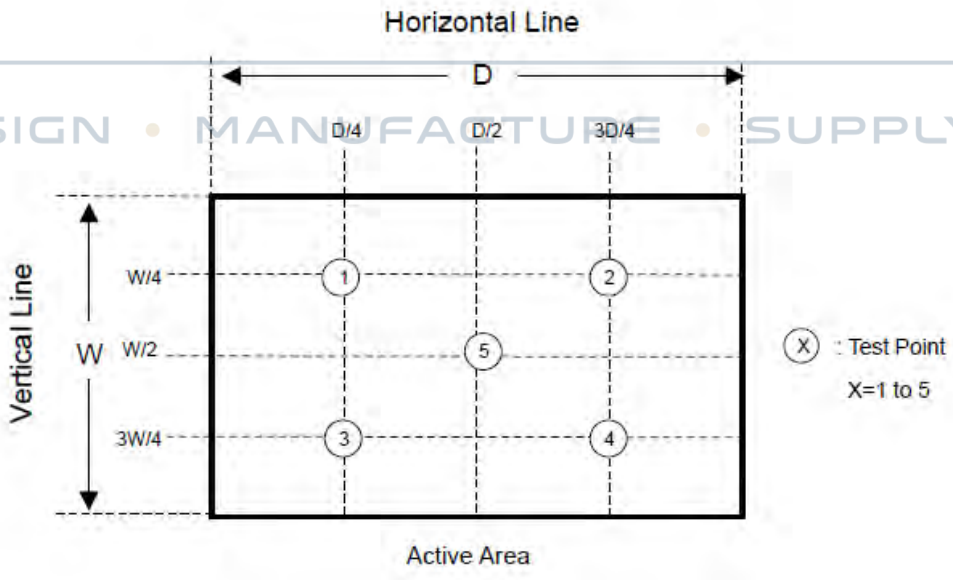
The output signals of photo detector are measured when the input signals are changed from “Full Black” to “Full White” (rising time), and from “Full White” to “Full Black” (falling time), respectively. The response time is interval between the 10% and 90% of amplitudes. Please refer to the figure as below.



Note 5: Color chromaticity and coordinates (CIE) is measured by Minolta CA210

Note 6: Center luminance is measured by Minolta CA210

Note 7: Luminance uniformity of these 5 points is defined as below and measured by Minolta CA210



Uniformity = (Min. Luminance of 5 points) / (Max. Luminance of 5 points)

3. Absolute Maximum Ratings

Absolute maximum ratings of the module are as following:

3.1 TFT LCD module

Items	Symbol	Min	Max	Unit	Conditions
Logic supply voltage	V_{DD}	-0.3	12	Volt	Note 1, 2

3.2 Backlight unit

Items	Symbol	Min	Max	Unit	Conditions
BLU input voltage			26.4	V	

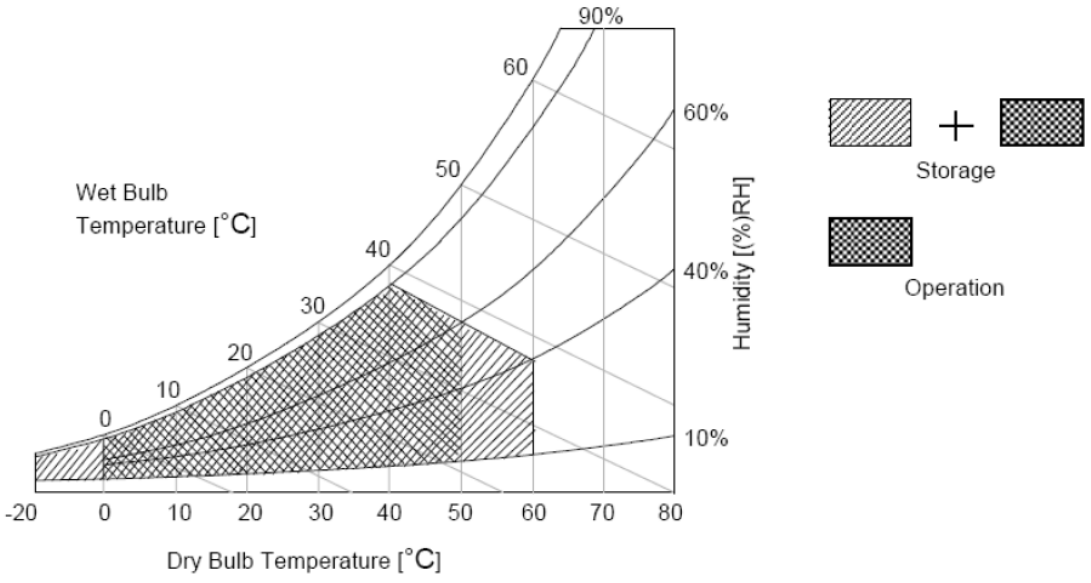
3.3 Environment

Items	Symbol	Values			Unit	Conditions
		Min.	Typ.	Max.		
Operation temperature	T_{OP}	-10	-	50	^{0}C	Note 3
Operation Humidity	H_{OP}	10		85	%	
Storage temperature	T_{ST}	-20		60	^{0}C	
Storage Humidity	H_{ST}	5		90	%	

Note 1: With in Ta= 25℃

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to IIS (Incoming Inspection Standard).



4. Interface specification

4.1 Input power

Parameter	Symbol	Values			Unit	Notes
		Min	Typ	Max		
MODULE :						
Power Supply Input Voltage	V_{LCD}	9.5	10.0	10.5	Vdc	5
Permissive Power Input Ripple	V_{dRF}			400	mV_{p-p}	1
Power Supply Input Current	I_{LCD}	-	(660)	(825)	mA	2
		-	(920)	(1150)	mA	3
Power Consumption	$P_{C\ TYP}$	-	(6.6)	(8.25)	Watt	2
	$P_{C\ MAX}$	-	(9.2)	(11.5)	Watt	3
Rush current	I_{RUSH}	-		3	A	4

Note :

1. Permissive power ripple should be measured under the condition of V_{LCD}=10.0V, 25°C,* f_V=60Hz
   Refer to page 7 for the pattern and more information.

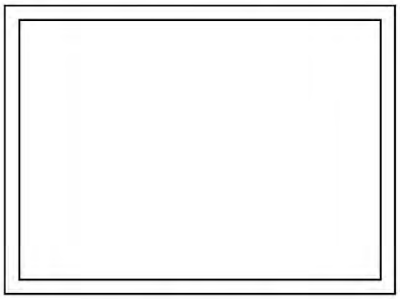
2. The specified current and power consumption can be measured under the V_{LCD}=10.0V, 25°C, f_V=60Hz and the pattern should be changed according to the typical or maximum power condition.
   The Max current can be measured only with the maximum power pattern.
   See the page 7 for details.

3. Maximum Condition of Inrush current :
   The duration of rush current is about 5ms and rising time of power Input is 500us ± 20%. (min.).

4. V_{LCD} level must be measured between two points on PCB of LCM (V_{LCD} (test point) ~ LCM Ground)
   (Test condition : maximum power pattern, 25°C, f_V=60Hz)

*fv=frame frequency

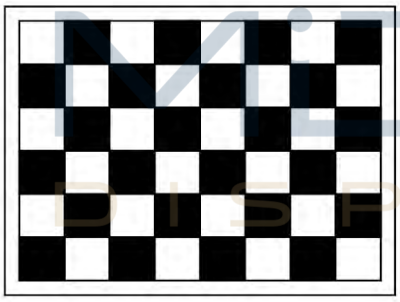
• **Permissive Power input ripple** (V_{LCD} =10.0V, 25°C, fv (frame frequency)=MAX condition)



White pattern

For the exact ripple measurement, the condition of Max 20Mhz is recommended in the Bandwidth configuration of oscilloscope.

• **Power consumption** (V_{LCD} =10V, 25°C, fv (frame frequency=60Hz condition)



Typical power Pattern

Maximum power Pattern

4.2 Backlight unit

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks (Test Condition)
Input Specification						
Input Voltage	**V_{in}**	21.6	24.0	26.4	V_{DC}	Input voltage: 24 V_{DC}
Input Current	**I_{in}**		4.5		A_{DC}	
BLU power	**P_{BLU}**		108		W	
On/Off control	**ON/OFF**	3.3	-	5.0	V_{DC}	ON STATE
		-	0	0.8		OFF STATE
Dimming (Analog)	**DIM**		3.3	5.0	V_{DC}	Min. Brightness
			0			Max. Brightness
Dimming (PWM)	**DIM**	-	3.3	5.0	V_{DC}	High level
		-	0	-		Low level
		10		100	%	Dimming range
		200	300	500	Hz	Dimming frequency
BLU lifetime	**MTBF**		50,000		hr	

4.3 Interface connector

4.3.1 TFT connector(CN1)

- LCD Connector(CN1) : GT05Q-30S-H10-MN(LSMtron), HD2S030HA2(JAE), KN38B-30S-0.5H(HIROSE)
- Mating Connector : 20453-030T-## (Manufactured by I-PEX)

No	Symbol	Description	No	Symbol	Description
1	VLCD	Power Supply +10.0V	16	Lane0P	True Signal for Main Link 0
2	VLCD	Power Supply +10.0V	17	Lane0N	Component Signal for Main Link 0
3	VLCD	Power Supply +10.0V	18	GND	Ground
4	VLCD	Power Supply +10.0V	19	Lane1P	True Signal for Main Link 1
5	VLCD	Power Supply +10.0V	20	Lane1N	Component Signal for Main Link 1
6	NC	No connection	21	GND	Ground
7	GND	Ground	22	Lane2P	True Signal for Main Link 2
8	NC	No Connection(I2C serial interface for LCM)	23	Lane2N	Component Signal for Main Link 2
9	NC	No Connection(I2C serial interface for LCM)	24	GND	Ground
10	GND	Ground	25	Lane3P	True Signal for Main Link 3
11	HPD	Hot Plug Detect Signal	26	Lane3N	Component Signal for Main Link 3
12	GND	Ground	27	GND	Ground
13	AUX_CHN	Component Signal for Auxiliary Channel	28	GND	Ground
14	AUX_CHP	True Signal for Auxiliary Channel	29	NC	No Connection
15	GND	Ground	30	GND	Ground

Notes :
1. All GND(ground) pins should be connected together to the LCD module's metal frame.
2. All VLCD (input power) pins should be connected together.

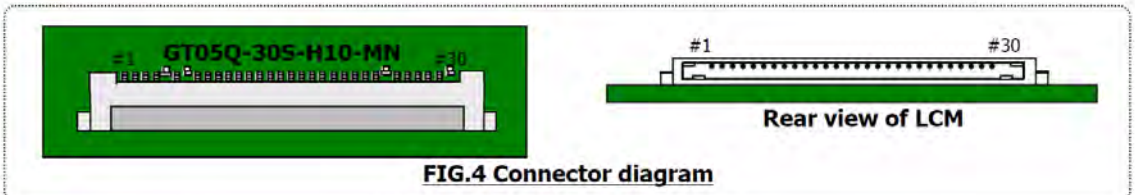


FIG.4 Connector diagram

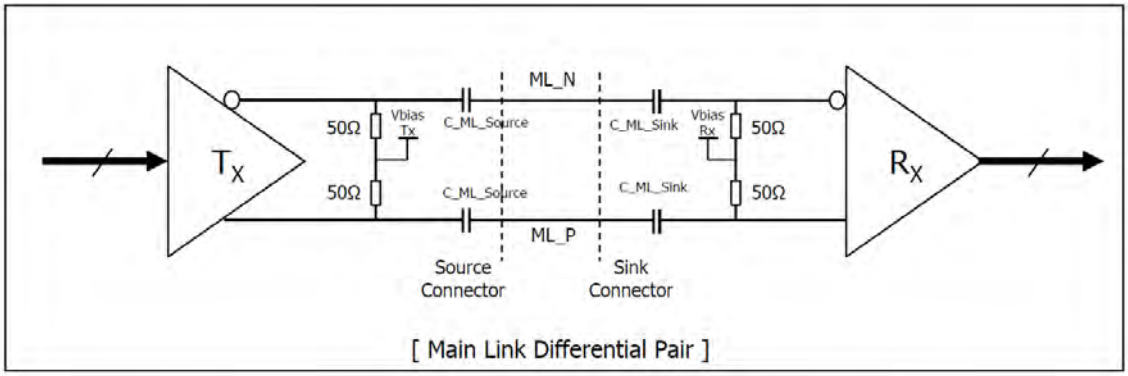
4.3.2 Backlight connector (CN2)

Connector: CviLux CI0114M1HR0 or equivalent

Pin NO	Symbol	Description
1	VIN	DC +24V
2	VIN	DC +24V
3	VIN	DC +24V
4	VIN	DC +24V
5	VIN	DC +24V
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	GND	Ground
10	GND	Ground
11	NC	No connected
12	ON / OFF	OFF=0V; ON=+5V
13	DIMM	20~100%
14	NC	No connected

4.4 eDP signal specifications

4.4.1 eDP main link signal

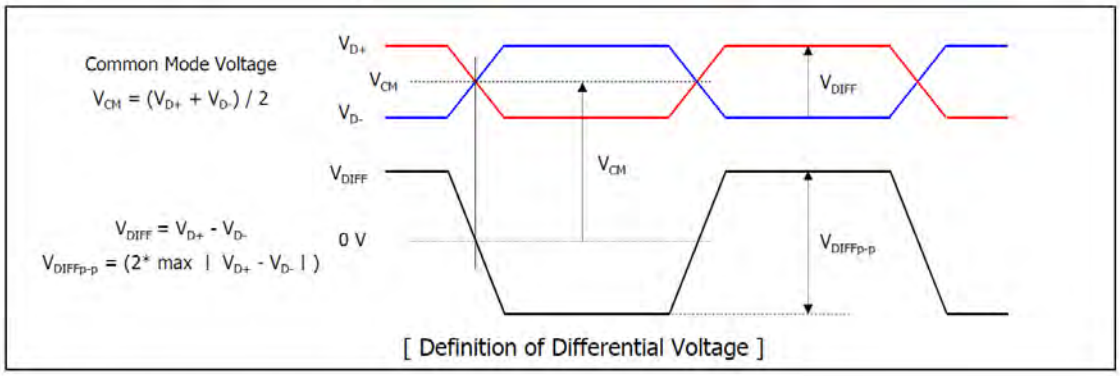


[Main Link Differential Pair]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval for high bit rate (5.4Gbps / lane)	UI_HBR2	-	185	-	ps	
Link Clock Down Spreading	Amplitude	0	-	0.5	%	
	Frequency	30		33	kHz	
Maximum output voltage level at Source side connector	$V_{TX-DIFFp-p-Max}$	-	-	1.38	V	Note 6)
Differential peak-to-peak voltage at Sink side connector	$V_{RX-DIFFp-p}$	0.09	-	-	V	Note 7)
EYE width at Sink side connector	$T_{RX-EYE-CONN}$	0.38	-	-	UI	Note 6,7)
Lane intra-pair skew	$L_{Rx-SKEW-INTRA\_PAIR}$	-	-	50	ps	
AC Coupling Capacitor	C_{SOURCE_ML}	75		200	nF	Source side

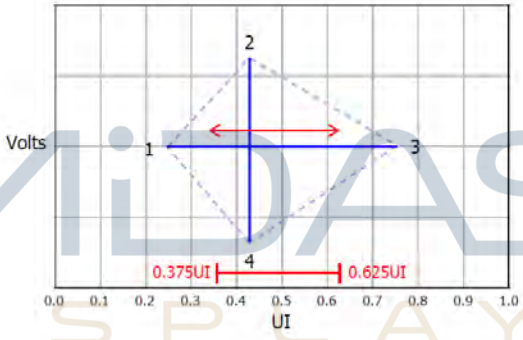
Notes:
1) In cabled embedded system, it is recommended the system designer ensure that EYE width and voltage are met at the sink side connector pins.
2) Mismatched common mode voltage will occur abnormal display.
3) All eDP electrical spec is measured at sink connector side.

Note6) Definition of Differential Voltage



[Definition of Differential Voltage]

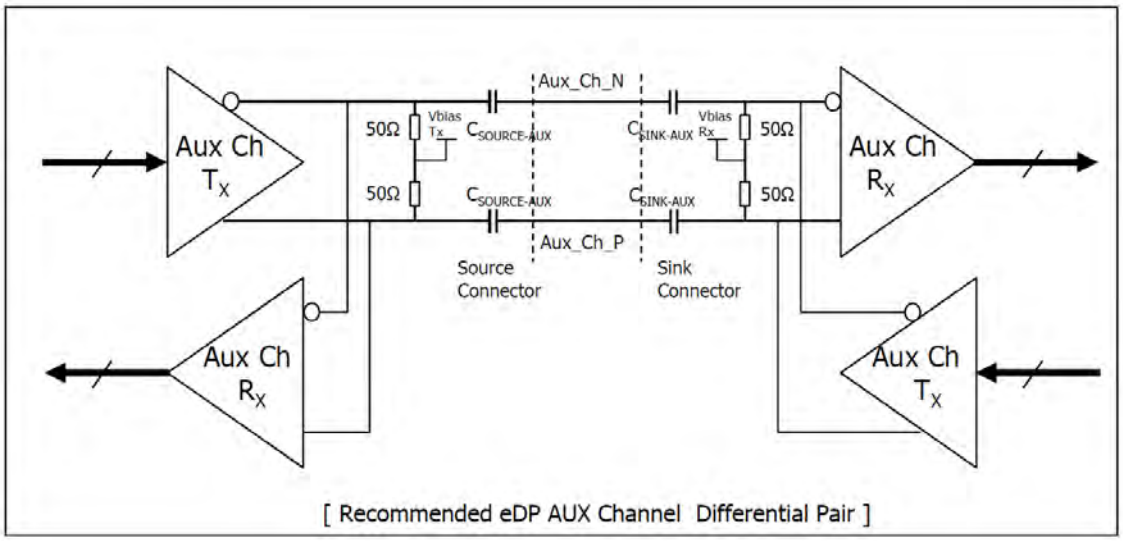
Note7) Main Link EYE Diagram



Point	High Bit Rate 2 @ TP3 EQ	
	Time(UI)	Voltage(V)
1	Any UI location (x) where the eye width is open from x to x+0.38UI	0.000
2	Any passing UI location between 0.375UI-0.625UI	0.045
3	Point 1 + 0.38UI	0.000
4	Same as Point 2	-0.045

[EYE Mask Vertices at embedded DP Sink Connector Pins]

4.4.2 eDP AUX channel signal

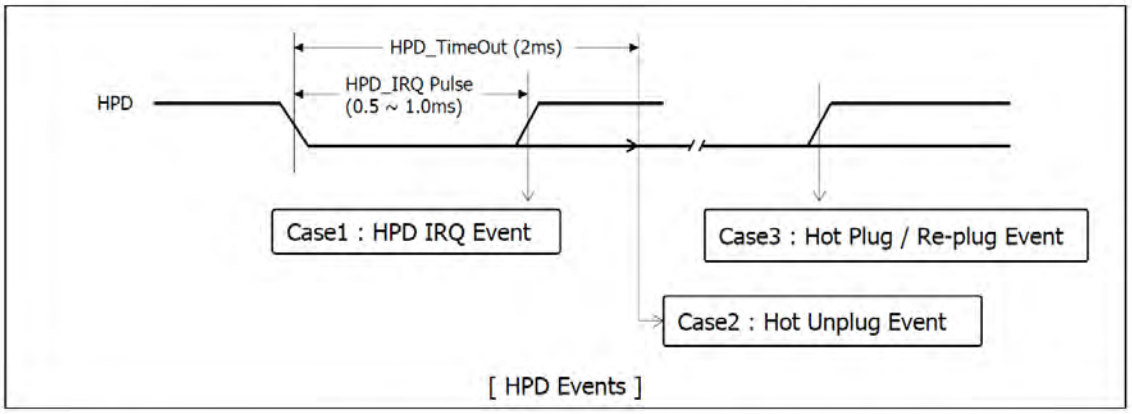


[Recommended eDP AUX Channel Differential Pair]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
AUX Unit Interval	UI	0.4	-	0.6	us	
AUX Jitter at Rx IC Package Pins	T_{jitter}	-	-	0.05	UI	Equal to 30ns
AUX Peak-to-peak voltage at Connector Pins of Receiving	$V_{AUX-DIFFp-p}$	0.32	-	1.36	V	
AUX Peak-to-peak voltage at Connector Pins of Transmitting		0.39	-	1.38	V	
AUX EYE width at Connector Pins of Tx and Rx		0.98	-	-	UI	
AUX AC Coupling Capacitor	$C_{SOURCE-AUX}$	75		200	nF	Source side

Notes:
1) $V_{AUX-DIFFp-p} = 2 * | V_{AUXP} - V_{AUXN} |$
2) Termination resistor should be 50ohm ± 5% at source side to AUX level.
3) Mismatched common mode voltage will occur abnormal display.

4.4.3 eDP HPD signal



[HPD Events]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
HPD Voltage	HPD	2.25	-	3.6	V	Sink side Driving
Hot Plug Detection Threshold		2.0	-	-	V	Source side Detecting
Hot Unplug Detection Threshold		-	-	0.8	V	
HPD_IRQ Pulse Width	HPD_IRQ	0.5	-	1.0	ms	
HPD_TimeOut		2.0	-	-	ms	HPD Unplug Event

Note)
1. HPD IRQ : Sink device wants to notify the Source device that Sink's status has changed so it toggles HPD line, forcing the Source device to read its Link / Sink Receiver DPCD field via the AUX-CH
2. HPD Unplug : The Sink device is no longer attached to the Source device and the Source device may then disable its Main Link as a power saving mode
3. Plug / Re-plug : The Sink device is now attached to the Source device, forcing the Source device to read its Receiver capabilities and Link / Sink status Receiver DPCD fields via the AUX-CH

4.5 Signal timing specifications

This is signal timing required at the input of the TMDS transmitter. All of the interface signal timing should be satisfied with the following specifications for it's proper operation.

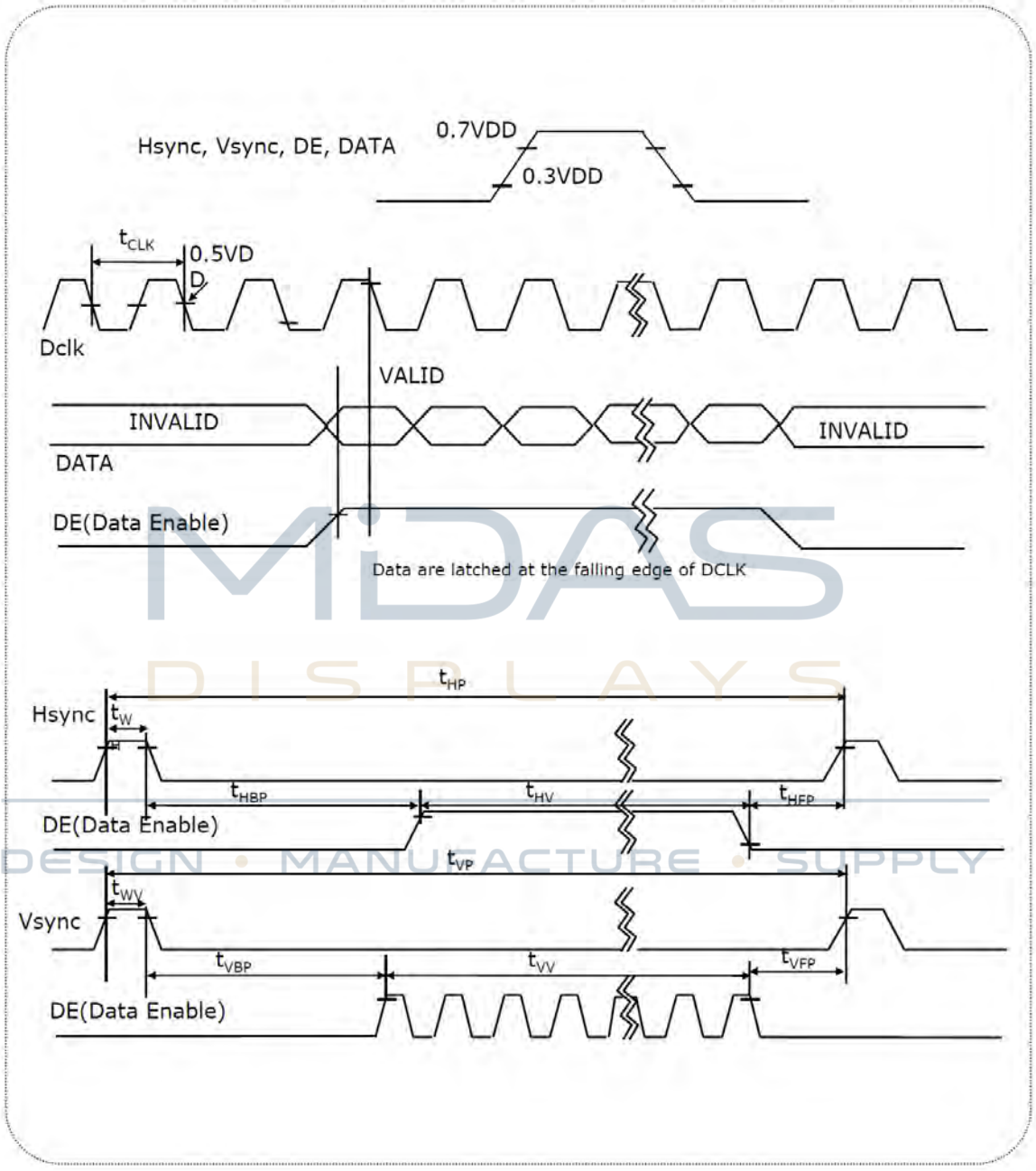
ITEM	Symbol		Min.	Typ.	Max.	Unit	Note
DCLK	Period	tCLK	1.82	1.875	1.93	ns	
	Frequency	-	518.25	533.25	548.25	MHz	
Hsync	Period	tHP	3968	4000	4040	tCLK	1,3,4
	Horizontal Valid	tHV	3840	3840	3840	tCLK	
	Horizontal Blank	tHB	128	160	192		
	Frequency	fH	129.2	133.3	139.9	KHz	
	Width	tWH	28	32	36	tCLK	
	Horizontal Back Porch	tHBP	52	80	108		
	Horizontal Front Porch	tHFP	48	48	48		
Vsync	Period	tVP	2220	2222	2268	tHP	2,4 *Adaptive sync: 40~60Hz
	Vertical Valid	tVV	2160	2160	2160	tHP	
	Vertical Blank	tVB	60	62	108	tHP	
	Frequency	fV	58.2	59.997	61.68	Hz	
	Width	tWV	5	5	5	tHP	
	Vertical Back Porch	tVBP	52	54	100		
	Vertical Front Porch	tVFP	3	3	3		

Notes :

1. The value of Hsync period, Hsync width and Hsync valid should be even number times of tCLK.
   If the value is odd number times of tCLK, it can make asynchronous signal timing and cause abnormal display.
2. The performance of the electro-optical characteristics may be influenced by variance of the vertical refresh rates.
3. The value of Hsync Period, Hsync Width, and Horizontal Back Porch should be divided by 4 without a remainder.
4. The polarity of Hsync, Vsync is not restricted.

* This panel supports adaptive sync timing(40~60Hz) only under moving picture in room temperature(25±5℃).
- It would not work usually under still image & reliability test.
- Under those condition, the phenomenon such as image sticking and flickering could be found on the screen.

4.6 Signal timing waveforms



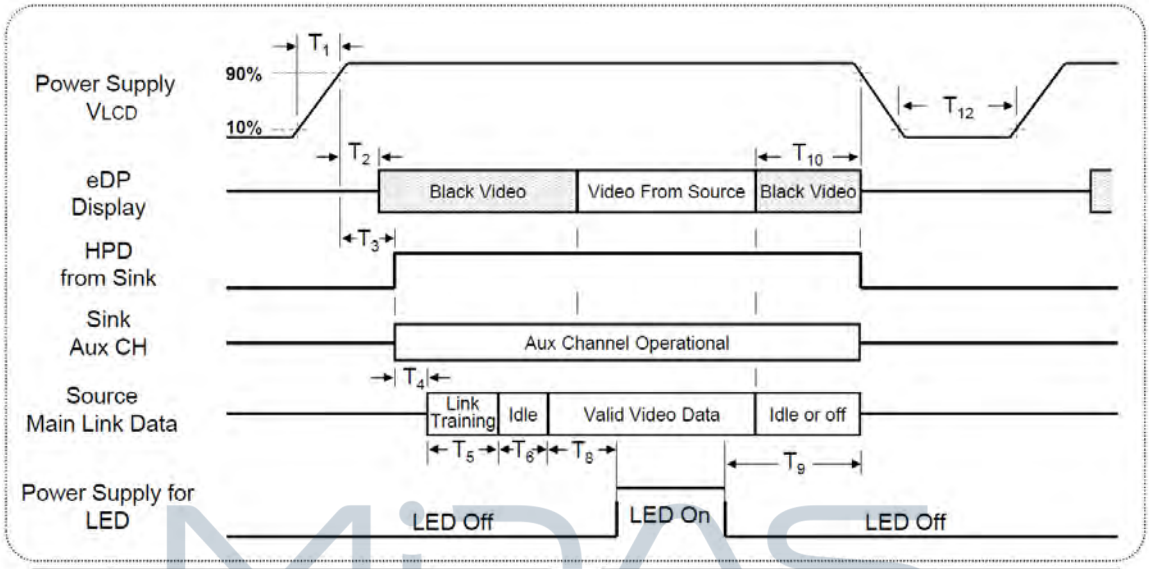
4.7 Color input data reference

The Brightness of each primary color(red,green,blue) is based on the 10-bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Color		Input Color Data		
		RED	GREEN	BLUE
		MSB LSB	MSB LSB	MSB LSB
		R9 R8 R7 R6 R5 R4 R3 R2 R1 R0	G9 G8 G7 G6 G5 G4 G3 G2 G1 G0	B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
Basic Color	Black	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
	Red (1023)	1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
	Green (1023)	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0
	Blue (1023)	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1
	Cyan	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1
	Magenta	1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1
	Yellow	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0
	White	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1
RED	RED (000)	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
	RED (001)	0 0 0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
	...	...	...	...
	RED (1022)	1 1 1 1 1 1 1 1 1 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
	RED (1023)	1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
GREEN	GREEN (000)	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
	GREEN (001)	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 0 0 0
	...	...	...	...
	GREEN (1022)	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 0	0 0 0 0 0 0 0 0 0 0
	GREEN (1023)	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0
BLUE	BLUE (000)	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
	BLUE (001)	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 1
	...	...	...	...
	BLUE (1022)	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 0
	BLUE (1023)	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1

4.8 Power sequence

4.8.1 Power sequence



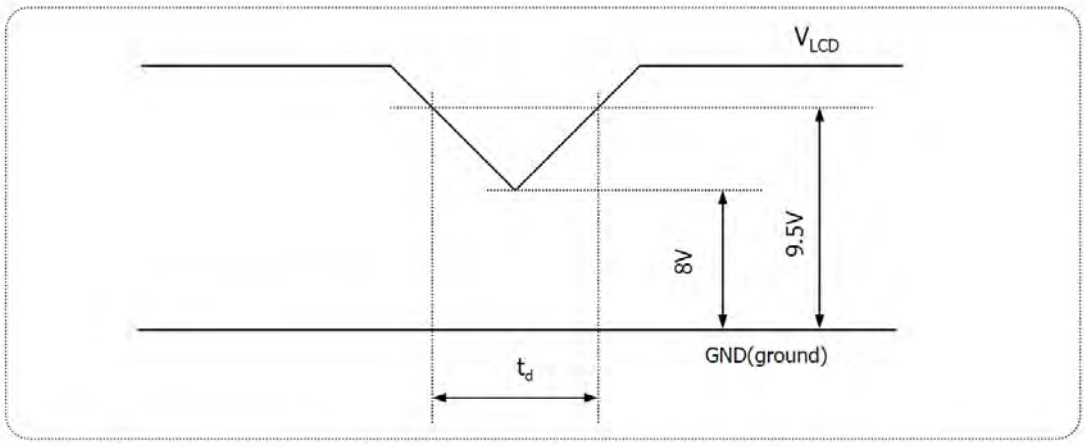
Timing	Required By	Limits		Units	Notes
		Min	Max		
T_1	Source	0.5	10	ms	
T_2	Sink	10	200	ms	
T_3	Sink	15	200	ms	
T_4	Source	-	-	ms	5
T_5	Source	-	-	ms	5
T_6	Source	-	100	ms	6
T_8	Source	350	-	ms	
T_9	Source	200	-	ms	4

Timing	Required By	Limits		Units	Notes
		Min	Max		
T_{10}	Source	0	500	ms	
T_{12}	Source	1000	-	ms	

Notes:

1) Power sequence should be kept all the time including below cases for normal operation.
   - AC/DC Power On/Off
   - Mode change (resolution, frequency, timing, sleep mode, color depth change, etc.)
   The violation of power sequence can cause a significant trouble in display and reliability.
2) Please avoid floating state of interface signal during signal invalid period.
3) When the interface signal is invalid, be sure to pull down the V_{LCD}.(0V)
4) Please turn off the power supply for LED when the level of V_{LCD} changes to prevent noise issue.
5) Link training duration is dependent on the customer's system.
6) It includes Source Frame Synchronization time.
   Source Frame Synchronization: Time to prepare before Tx(Source) sends valid data(Invalid period).

4.8.2 V_{LCD} power dip condition



For proper operation, stable power supply of V_{LCD} is necessary and power dip is allowed only in below condition.
Except this condition, power on/off should follow power sequence specification in page 18 exactly.

1) Dip condition

$8V \le V_{LCD} < 9.5V$, $t_d \le 20ms$

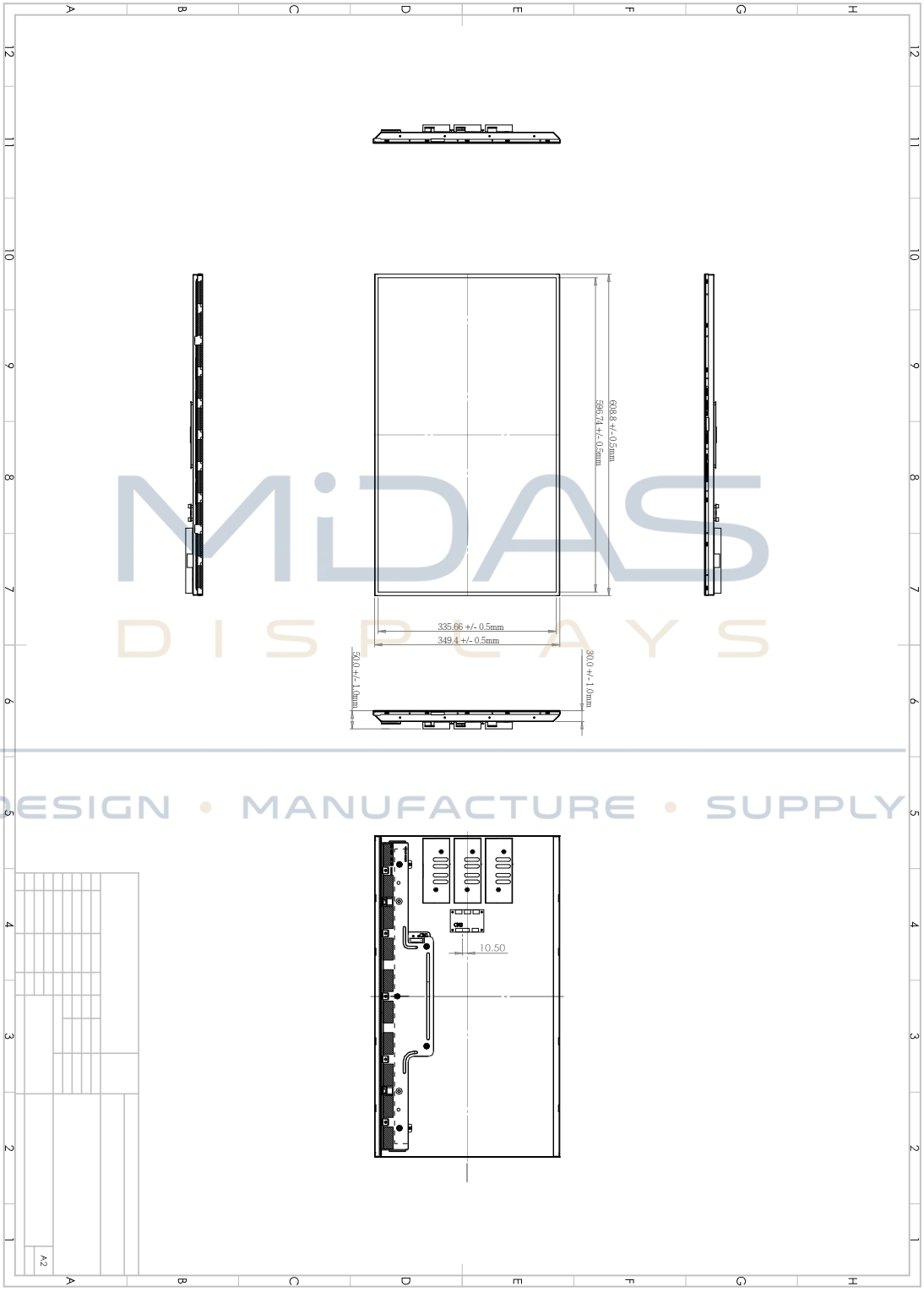
5. Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta=40℃, 80%RH, 240hours	
High Temperature Operation (HTO)	Ta= 50℃, 240hours	
Low Temperature Operation (LTO)	Ta= -10℃, 240hours	
High Temperature Storage (HTS)	Ta= 60℃, 240hours	
Low Temperature Storage (LTS)	Ta= -20℃, 240hours	

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -10℃ to 50℃, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

7. Mechanical Characteristics



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