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MDT430002C	1920x1080	LVDS Interface	TFT Module
Specification			
Version: 1		Date: 16/12/2021	
Revision			
1	14/12/2021	First issue	

Display Features	
Display Size	43”
Resolution	1920x1080
Orientation	Landscape
Appearance	RGB
Logic Voltage	12V
Interface	LVDS
Brightness	1400 cd/m^2
Touchscreen	CTP
Module Size	963.90 x 551.64 x 53.71 mm
Operating Temperature	-20°C ~ +60°C
Pinout	51 way connector
Pitch	0.50 mm

RoHS compliant

Created By	Checked By
CL	TSB
Box Quantity	Weight / Display
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Display Accessories	
Part Number	**Description**
MDIB-CC1	Interconnect board for standard pitch pinouts to fine pitch wires. Providing pinouts for 2.54 pinout. 1.27, 1, 0.845, 0.8, 0.7, 0.65, 0.62, 0.6, 0.5 & 0.3 pads.

Optional Variants	
Appearances	**Voltage**

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open or modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
10) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

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2. General Description

2.1 Overview

This specification applies to the Color Active Matrix Liquid Crystal Display composed of a TFT-LCD display a LED backlight system. The screen format is intended to support FHD (1920(H) x 1080(V)) screen and 16.7M colors.
The 24V LED backlight driving board is included.

2.2 Features

- High brightness display, 1400nits by direct LED backlight.
- High speed response
- Long operation lifetime BLU design
- RoHS Compliance
- High TNI 105℃ LC applied

2.3 Application

Industrial applications.

2.4 Display specifications

Items	Unit	Specification
Screen Diagonal	mm	42.5inch
Active Area	mm	940.896 (H) X 529.254(V)
Pixels H x V	pixels	1920 x3(RGB) x 1080
Pixels Pitch	um	490.05 (per one triad) x 490.05
Pixel Arrangement		RGB Vertical stripe
Display mode		Normally Black
White luminance (center)	Cd/m^2	1400 (Typ)
Contrast ratio		1200 : 1
Optical Response Time	msec	8 ms (Typ. On/off)
Normal Input Voltage VDD	Volt	12.0
Power Consumption (Vcc Line + LED backlight)	Watt	126W (VDD line=6 W; LED lines= 120 W)
Weight	Grams	TBD
Physical size	mm	963.9 (W)×551.64 (H)×53.71 (D)
Electrical Interface		LVDS
Support colors		16.7M colors
Surface Treatment		Anti-glare and hard-coating 3H
Temperature range		
Operating	^0C	-20 ~ 60
Storage	^0C	-20 ~ 60
RoHS Compliance		RoHS Compliance

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2.5 Optical characteristics

The following optical characteristics are measured under stable condition at 25 ^{0}C

Items	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing angle	Deg.	Horizontal (Right)		89		2
		CR=10 (Left)		89		
		Vertical (Up)		89		
		CR=10 (Down)		89		
Contrast Ratio		Normal Direction		1200		3
Response Time	msec	Raising + Falling		8	10	4
Color / Chromaticity Coordinates (CIE)		Red x	-0.05	0.646	+0.05	5
		Red y		0.300		
		Green x		0.318		
		Green y		0.507		
		Blue x		0.144		
		Blue y		0.056		
Color coordinates (CIE) White		White x		0.320		
		White y		0.342		
Center Luminance	Cd/m^2		1200	1400		6
Luminance Uniformity	%		70	75		7
Crosstalk (in 60 Hz)	%				1.5	
Flicker	dB				-20	

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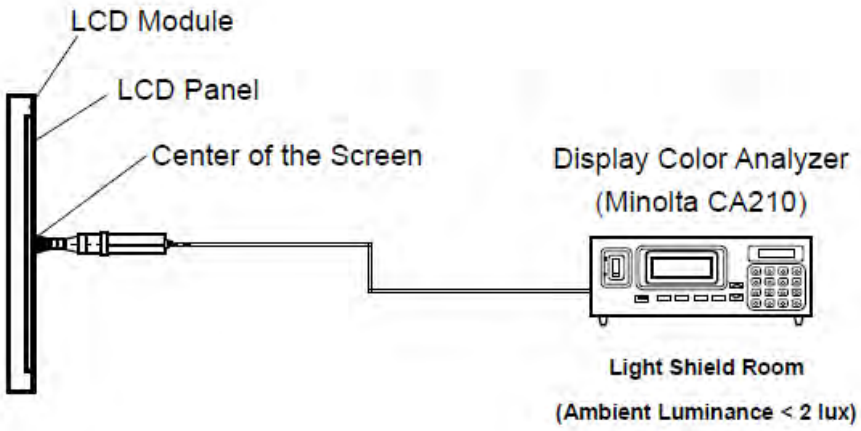
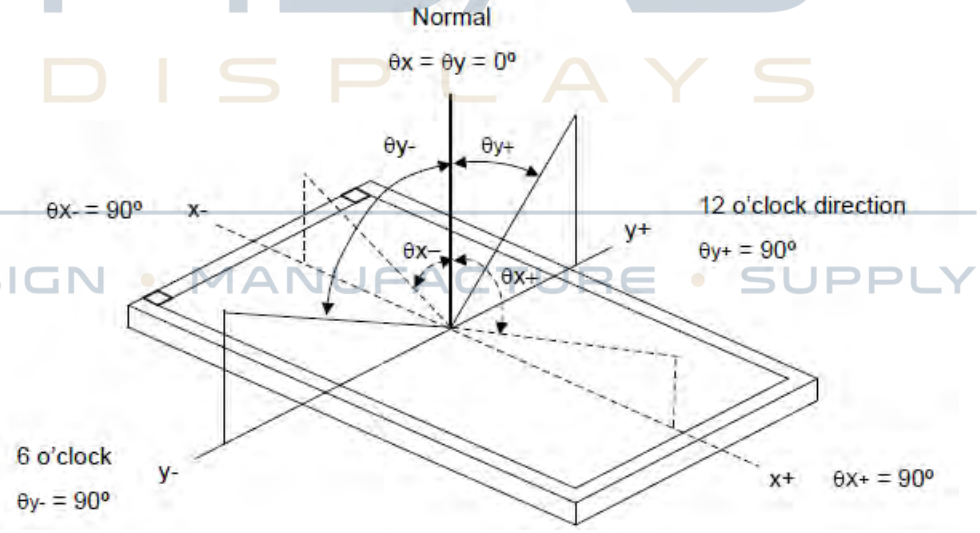
Note 1: Measurement method

The LCD module should be stabilized at given temperature for 0.5 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.



Note 2: Definition of viewing angle



Note 3: Contrast ratio is measured by Minolta CA210

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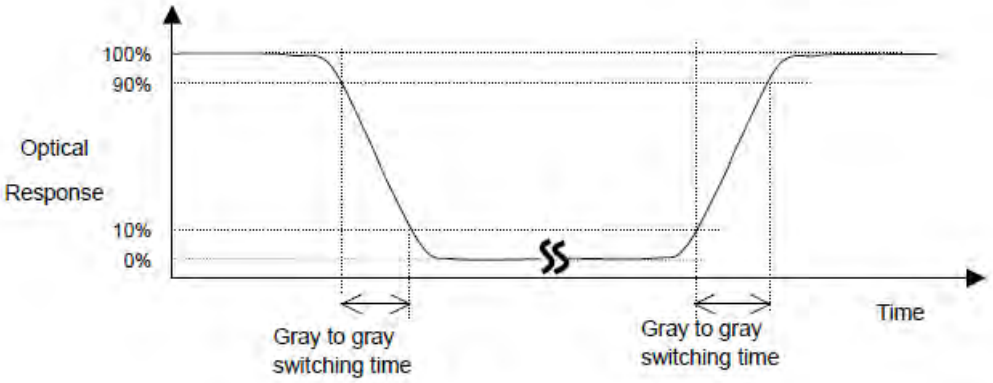
Note 4: Definition of Response time

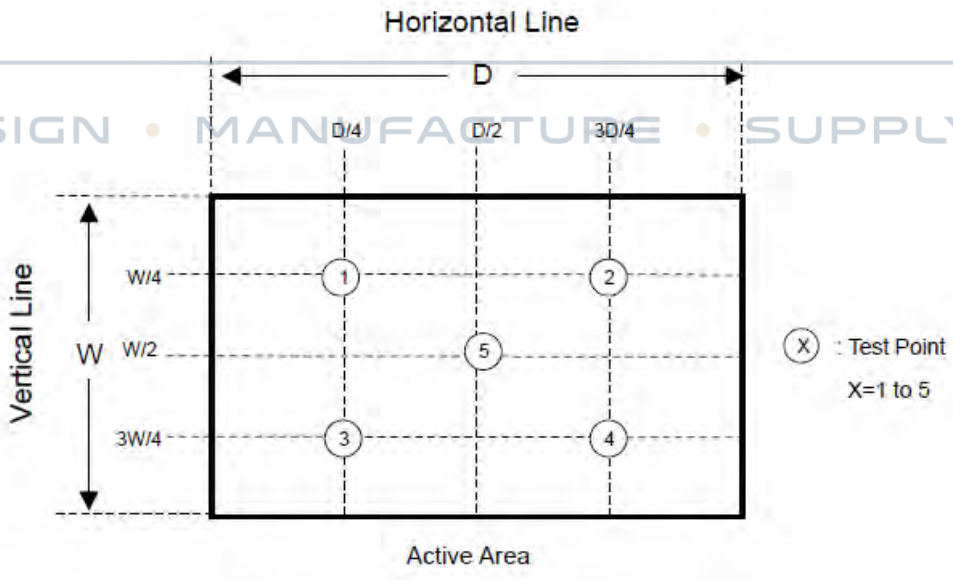
The output signals of photo detector are measured when the input signals are changed from “Full Black” to “Full White” (rising time), and from “Full White” to “Full Black” (falling time), respectively. The response time is interval between the 10% and 90% of amplitudes. Please refer to the figure as below.



Note 5: Color chromaticity and coordinates (CIE) is measured by Minolta CA210

Note 6: Center luminance is measured by Minolta CA210

Note 7: Luminance uniformity of these 5 points is defined as below and measured by Minolta CA210



Uniformity = (Min. Luminance of 5 points) / (Max. Luminance of 5 points)

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3. Absolute Maximum Ratings

Absolute maximum ratings of the module are as following:

3.1 TFT LCD module

Items	Symbol	Min	Max	Unit	Conditions
Logic supply voltage	V_{DD}	V_{SS}-0.3	13.5	Volt	Note 1, 2

3.2 Backlight unit

Items	Symbol	Min	Max	Unit	Conditions
BLU input voltage			26.4	V	

3.3 Environment

Items	Symbol	Values			Unit	Conditions
		Min.	Typ.	Max.		
Operation temperature	T_{OP}	-20	-	60	^{0}C	Note 3
Operation Humidity	H_{OP}	10		80	%	
Storage temperature	T_{ST}	-20		60	^{0}C	
Storage Humidity	H_{ST}	10		80	%	

Note 1: With in Ta= 25℃

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to IIS (Incoming Inspection Standard).

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4. Interface specification

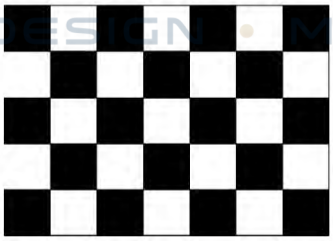
4.1 Input power

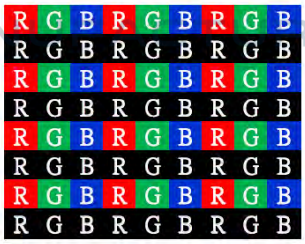
[Ta =25±2℃]

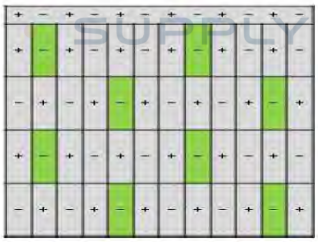
Parameter		Symbol	Values			Unit	Remark
			Min	Typ	Max		
Power Supply Input Voltage		VDD	10.8	12	13.2	Vdc	
Power Supply Ripple Voltage		VRP			300	mV	
Power Supply Current		IDD	-	500	950	mA	Note 1
Power Consumption		PDD	-	6	11.4	Watt	
Rush current		IRUSH	-	-	3.0	A	Note 2
LVDS Interface	Differential Input High Threshold Voltage	VLVTH	+100		+300	mV	
	Differential Input Low Threshold Voltage	VLVTL	-300		-100	mV	
	Common Input Voltage	VLVC	1.0	1.2	1.4	V	
CMOS Interface	Input High Threshold Voltage	VIH	2.7	-	3.3	V	
	Input Low Threshold Voltage	VIL	0	-	0.6	V	

Note 1 : The supply voltage is measured and specified at the interface connector of LCM.
The current draw and power consumption specified is for VDD=12.0V,
Frame rate f_V=60Hz and Clock frequency = 74.25MHz.
Test Pattern of power supply current

a) Typ : Mosaic 7X5 (L0/L255) b) Max : Horizontal 1 Line (L0/L255)) c) Flicker Pattern







Note 2 : The duration of rush current is about 2ms and rising time of Power Input is 1ms(min)

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4.2 Backlight unit

Parameter	Symbol	Min	Typ.	Max	Unit	Remarks (Test condition)
Input Voltage	Vin	21.6	24.0	26.4	V_{DC}	
Input current	Iin		5.0		A	Vin=24V, Dim=max
BLU power			120		W	
On/Off control	ON/OFF		3.3	5	V_{DC}	ON state
		-0.3		0.7		OFF state
Dimming control	DIMM	180	200	220	Hz	PWM
BLU lifetime			100,000		hrs	

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4.3 Interface connector

4.3.1 TFT connector(CN1)

- LVDS Connector : PM.LVS.S040505101(UJC) 、IS050-C51B-C39-S(UJU) or 0.5Ph H3.75 LVDS(DEREN).

Pin No	Symbol	Description	Pin No	Symbol	Description
1	NC	No Connection	21	GND	Ground
2	SDA	I²C Data	22	CH1[3]-	First pixel negative LVDS differential data input. Pair3
3	SCL	I²C Clock	23	CH1[3]+	First pixel positive LVDS differential data input. Pair3
4	NC	Not Connected	24	NC	Not Connected
5	NC	Not Connected	25	NC	Not Connected
6	NC	Not Connected	26	NC	Not Connected
7	SELLVDS	High: JEIDA Low or Open: VESA	27	NC	Not Connected
8	NC	Not Connected	28	CH2[0]-	Second pixel negative LVDS differential data input. Pair0
9	NC	Not Connected	29	CH2[0]+	Second pixel positive LVDS differential data input. Pair0
10	NC	Not Connected	30	CH2[1]-	Second pixel negative LVDS differential data input. Pair1
11	GND	Ground	31	CH2[1]+	Second pixel positive LVDS differential data input. Pair1
12	CH1[0]-	First pixel negative LVDS differential data input. Pair0	32	CH2[2]-	Second pixel negative LVDS differential data input. Pair2
13	CH1[0]+	First pixel positive LVDS differential data input. Pair0	33	CH2[2]+	Second pixel positive LVDS differential data input. Pair2
14	CH1[1]-	First pixel negative LVDS differential data input. Pair1	34	GND	Ground
15	CH1[1]+	First pixel positive LVDS differential data input. Pair1	35	CH2CLK-	Second pixel negative LVDS clock
16	CH1[2]-	First pixel negative LVDS differential data input. Pair2	36	CH2CLK+	Second pixel positive LVDS clock
17	CH1[2]+	First pixel positive LVDS differential data input. Pair2	37	GND	Ground
18	GND	Ground	38	CH2[3]-	Second pixel negative LVDS differential data input. Pair3
19	CH1CLK-	First pixel negative LVDS clock	39	CH2[3]+	Second pixel positive LVDS differential data input. Pair3
20	CH1CLK+	First pixel positive LVDS clock			

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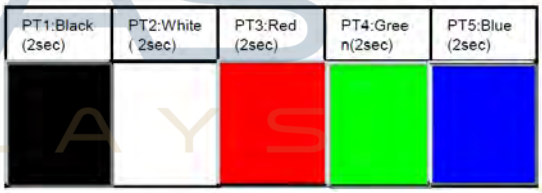
Pin No	Symbol	Description	Pin No	Symbol	Description
40	NC	Not Connected	46	GND	Ground
41	NC	Not Connected	47	NC	Not Connected
42	NC	Not Connected	48	VCC	Input Voltage +12V
43	NC	Not Connected	49	VCC	Input Voltage +12V
44	GND	Ground	50	VCC	Input Voltage +12V
45	GND	Ground	51	VCC	Input Voltage +12V

Notes :

1. NC(Not Connected) : This pins are only used for internal operations.
2. Input Level of LVDS signal is based on the EIA-644 Standard.
3. LVDS_SEL: This pin is used for selecting LVDS signal data format.
   If this Pin : High (3.3V) ==>JEIDA LVDS format
   Otherwise : Low(GND) or Open (NC) ==>Normal NS LVDS format

Rear view of LCM

BIST Pattern



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4.3.2 Backlight connector(CN2)

Connector: CviLux CI0114M1HR0 or equivalent

Pin NO	Symbol	Description
1	VIN	DC +24V
2	VIN	DC +24V
3	VIN	DC +24V
4	VIN	DC +24V
5	VIN	DC +24V
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	GND	Ground
10	GND	Ground
11	NC	No connected
12	ON / OFF	OFF=0V; ON=+5V
13	DIMM	20~100%
14	NC	No connected

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4.4 LVDS interface

- LVDS Receiver : Timing Controller (LVDS Rx merged) / LVDS Data : Pixel Data

Channel No.	Data No.	8-bit LVDS Type	
		NS	JEIDA
0	Bit-0	R0	R2
	Bit-1	R1	R3
	Bit-2	R2	R4
	Bit-3	R3	R5
	Bit-4	R4	R6
	Bit-5	R5	R7
	Bit-6	G0	G2
1	Bit-0	G1	G3
	Bit-1	G2	G4
	Bit-2	G3	G5
	Bit-3	G4	G6
	Bit-4	G5	G7
	Bit-5	B0	B2
	Bit-6	B1	B3
2	Bit-0	B2	B4
	Bit-1	B3	B5
	Bit-2	B4	B6
	Bit-3	B5	B7
	Bit-4	HS	HS
	Bit-5	VS	VS
	Bit-6	DE	DE
3	Bit-0	R6	R0
	Bit-1	R7	R1
	Bit-2	G6	G0
	Bit-3	G7	G1
	Bit-4	B6	B0
	Bit-5	B7	B1
	Bit-6	-	

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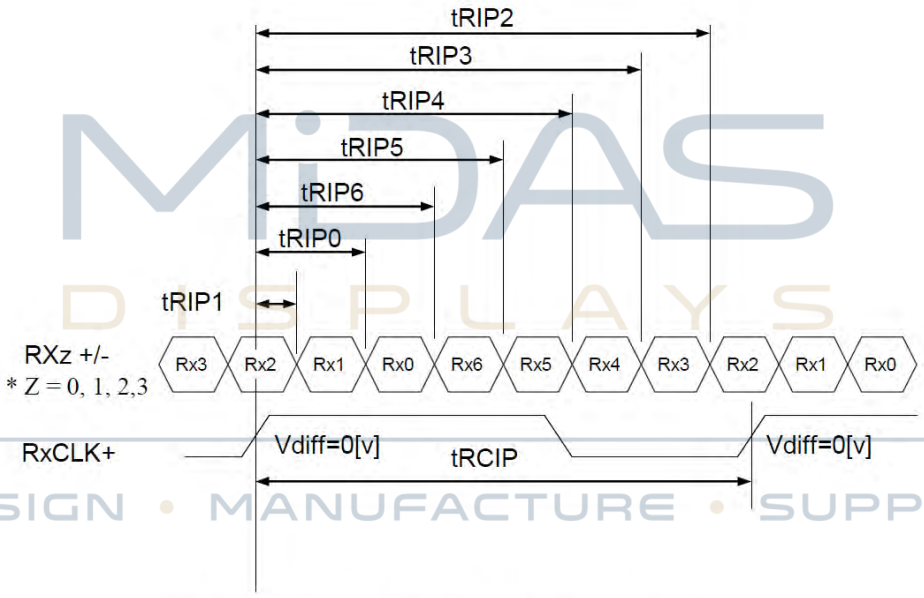
4.5 LVDS Rx interface timing parameter

The specification of the LVDS Rx interface timing parameter is shown below.

Item	Symbol	Min	Typ	Max	Unit	Remark
CLKIN Period	tRCIP	10.31	13.47(10.78)	15.87	nsec	
Input Data 0	tRIP1	-0.42	0.0	+0.42	nsec	
Input Data 1	tRIP0	tRCIP/7-0.42	tRCIP/7	tRCIP/7+0.42	nsec	
Input Data 2	tRIP6	2 ×tRCIP/7-0.42	2 ×tRCIP/7	2 ×tRCIP/7+0.42	nsec	
Input Data 3	tRIP5	3 ×tRCIP/7-0.42	3 ×tRCIP/7	3 ×tRCIP/7+0.42	nsec	
Input Data 4	tRIP4	4 ×tRCIP/7-0.42	4 ×tRCIP/7	4 ×tRCIP/7+0.42	nsec	
Input Data 5	tRIP3	5 ×tRCIP/7-0.42	5 ×tRCIP/7	5 ×tRCIP/7+0.42	nsec	
Input Data 6	tRIP2	6 ×tRCIP/7-0.42	6 ×tRCIP/7	6 ×tRCIP/7+0.42	nsec	



* Vdiff = (RXz+)-(RXz-),…. ,(RXCLK+)-(RXCLK-)

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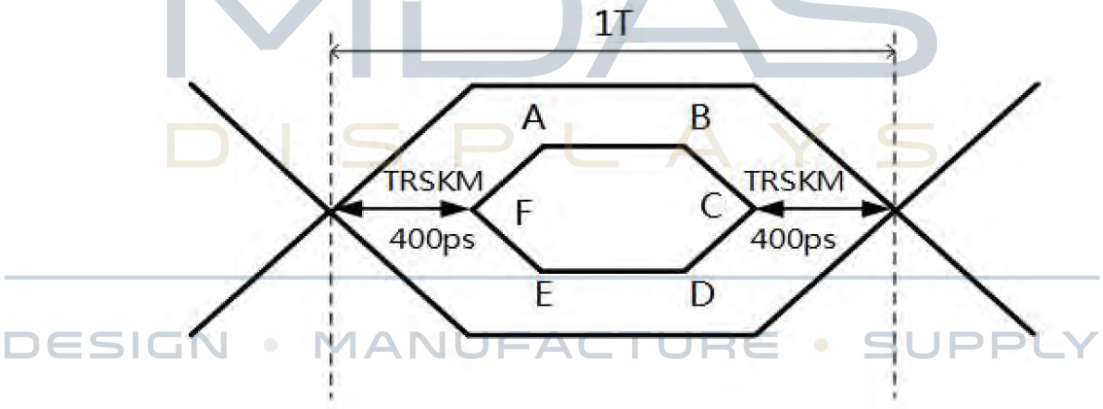
4.6 LVDS Rx interface eye diagram

Symbol	Min	Typ	Max	Unit	Note
A	–	100	–	mV	
B	–	100	–	mV	
C	–	0	–	mV	
D	–	-100	–	mV	
E	–	-100	–	mV	
F	–	0	–	mV	



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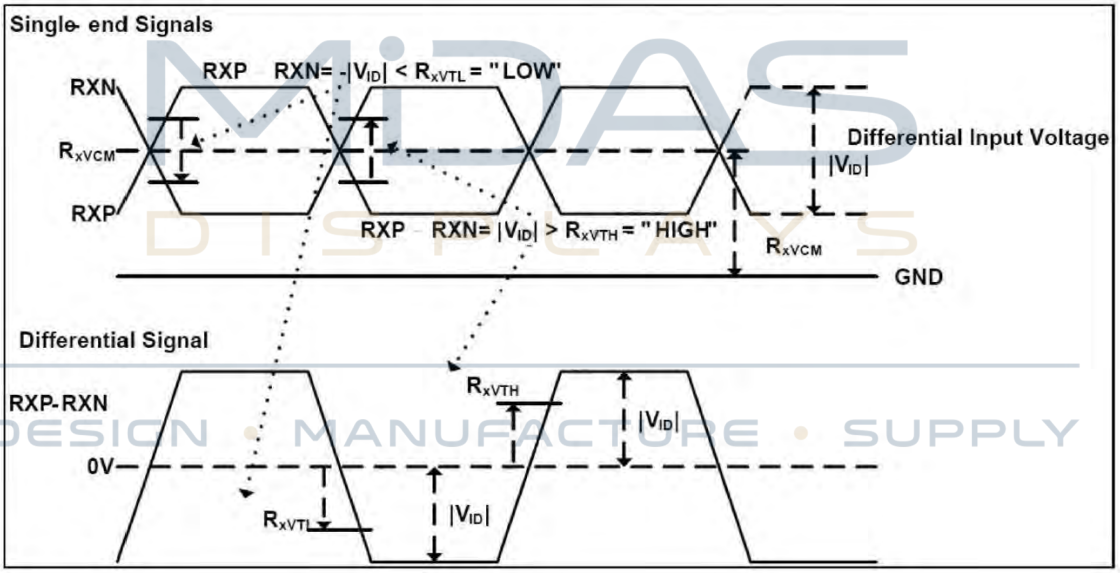
Notes: 1. Time F to A,B to C,C to D,E to F is 150p second.
2. LVDS clock=85Mhz.
3. The time A to B=1T-2*TRSKM-2*150ps.

4.7 LVDS receiver differential input

Symbol	Parameter	Min	Typ	Max	Unit	Condition
R_{xVTH}	Differential input high threshold voltage			+0.1v	V	RxVCM =1.2V
R_{xVTL}	Differential input low threshold voltage	-0.1V			V	
R_{XVIN}	Input voltage range (singled-end)	0		2.4	V	
R_{xVCM}	Differential input common mode voltage	$\|V_{ID}\|/2$		2.4-$\|V_{ID}\|/2$	V	
$\|V_{ID}\|$	Differential input voltage	0.1		0.6	V	



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5. Signal timing specification

5.1 Timing parameters (DE only mode)

Item		Symbols		Min	Typ	Max	Unit
Clock	Frequency	1/Tc		60	74.25	78	MHz
	High Time	Tch		-	4/7Tc	-	
	Low Time	Tcl		-	4/7Tc	-	
Frame Period		Tv		1100	1125	1149	lines
				48.5	60	63	Hz
Horizontal Active Display Term		Valid	t_{HV}	-	960	-	t_{CLK}
		Total	t_{HP}	1060	1100	1200	t_{CLK}
Vertical Active Display Term		Valid	t_{VV}	-	1080	-	t_{HP}
		Total	t_{VP}	1100	1125	1149	t_{HP}

Notes: This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F	LVDS Input frequency	-	45	74.25	85	MHz
T_{LVSK}	LVDS channel to channel skew	F=100MHz V_{IC}=1.2V V_{ID}=±400mV	-380	-	+380	ps
F_{LVMOD}	Modulating frequency of input clock during SSC		-	-	85	KHz
F_{LVDEV}	Maximum deviation of input clock frequency during SSC		-3	-	+3	%
T_{CY-CY}	Cycle to Cycle jitter		-	-	100	ps

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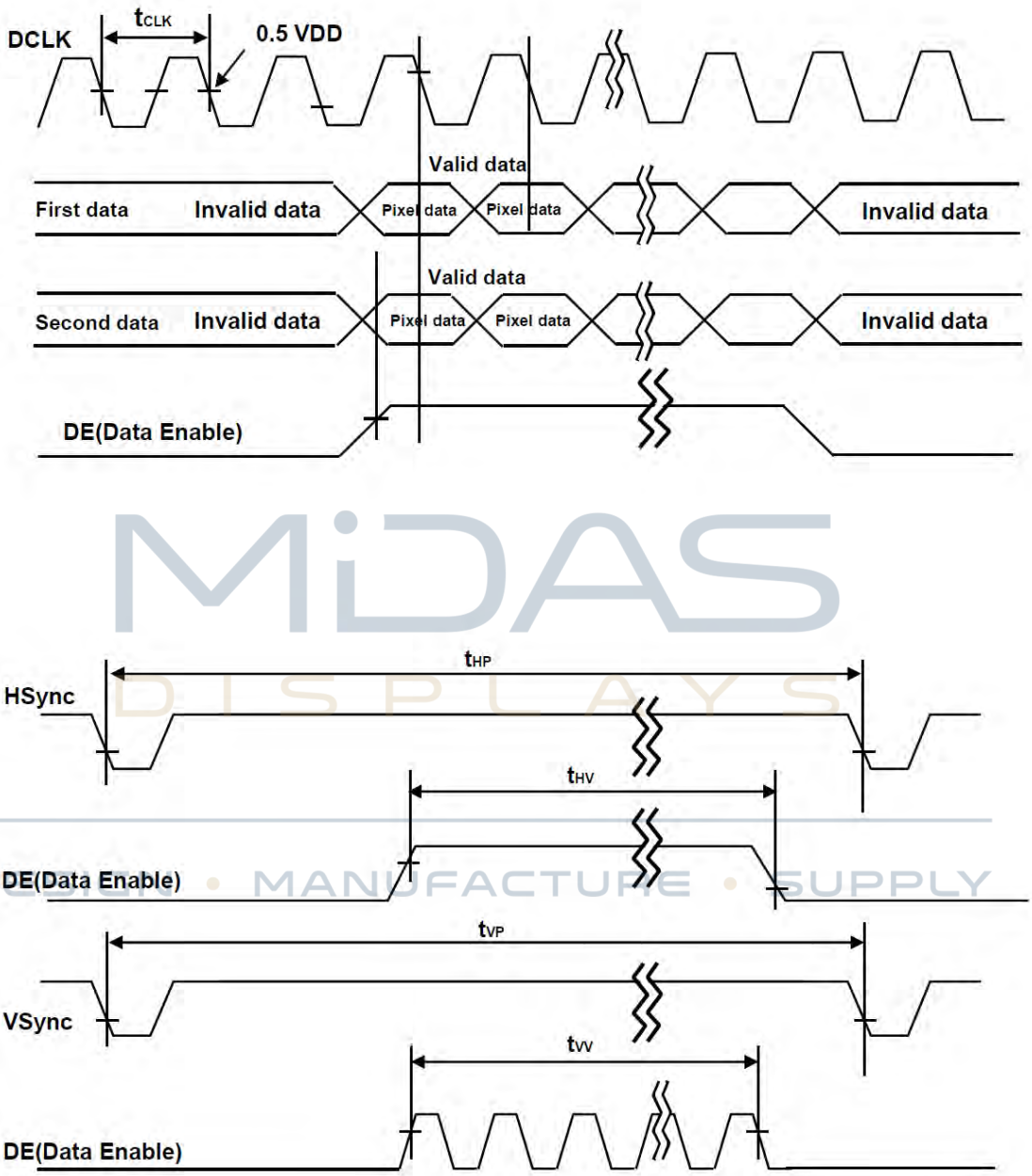
5.2 Signal timing waveform



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5.3 Input signals, basic display colors and gray scale of colors

Color & Gray Scale		Input Data Signal																							
		Red Data								Green Data								Blue Data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▽	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	▽	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	▽	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Gray Scale of White	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1
	▽	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

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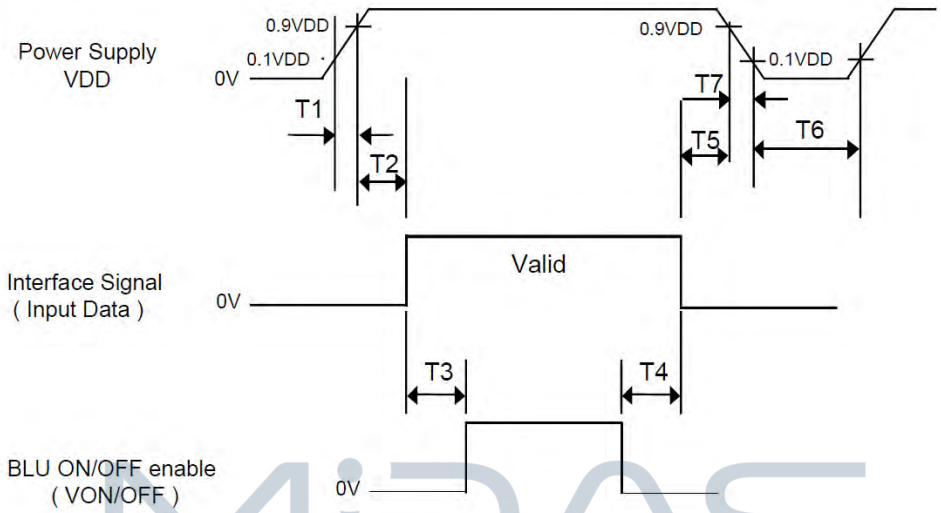
5.4 Power sequence

To prevent a latch-up or DC operation of the Open Cell, the power on/off sequence shall be as shown in below



Parameter	Values			Units
	Min	Typ	Max	
T1	0.5	-	20	ms
T2	10	-	100	ms
T3	200	-	-	ms
T4	200	-	-	ms
T5	0	-	-	ms
T6	1	-	-	s

Notes: 1. Back Light must be turn on after power for logic and interface signal are valid.
2. Even though T1 is out of SPEC, it is still ok if the inrush current of VDD is below the limit.
3. When VDD<0.9VDD(Typ.),Power off.
4. T7 decreases smoothly, if there were rebounding voltage, it must smaller than 5 volts.

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6. Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta=40℃, 80%RH, 240hours	
High Temperature Operation (HTO)	Ta= 60℃, 240hours	3
Low Temperature Operation (LTO)	Ta= -20℃, 240hours	
High Temperature Storage (HTS)	Ta= 60℃, 240hours	
Low Temperature Storage (LTS)	Ta= -20℃, 240hours	
Thermal Shock Test (TST)	-20℃/30min, 60℃/30min, 100 cycles	
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (ElectroStatic Discharge)	Contact Discharge: ± 8KV, 150pF(330Ω) 1sec, 9 points, 25 times/ point.	
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 9 points, 25 times/ point.	

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -10℃ to 50℃, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.

Note 3: TFT surface.

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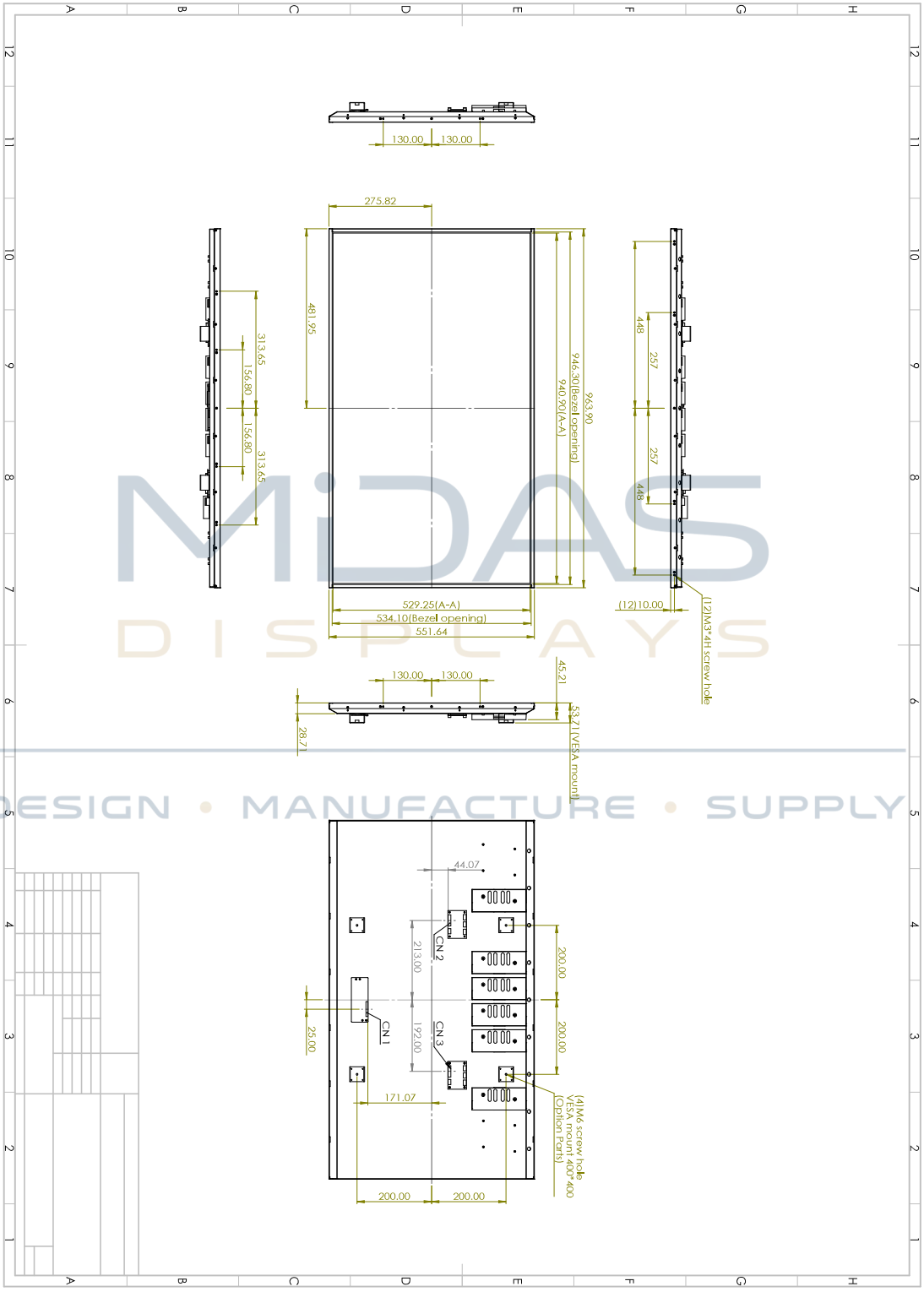
8. Mechanical Characteristics



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